

A Modified Carrier-Based PWM Technique for Cascaded H-Bridge Inverters: Enhanced Harmonic Reduction and DC Bus Utilization

Syafirul Imran Shaharuddin¹, Fazlli Patkar^{1*}, Jurifa Mat Lazi¹, Md Hairul Nizam Talib¹, Azrita Alias¹, Nurul Ain Said¹, Zainuddin Mat Isa²

¹Fakulti Teknologi dan Kejuruteraan Elektrik, Universiti Teknikal Malaysia Melaka, Melaka, Malaysia

²Fakulti Kejuruteraan dan Teknologi Elektrik, Universiti Malaysia Perlis, Perlis, Malaysia

Email: *fazlli@utem.edu.my

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Abstract

Multilevel inverters are a crucial component in renewable energy systems, motor drives, and grid system due to their capability to generate high-quality AC output power. Among various multilevel inverter topologies, Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is known for its scalability and modularity. However, the main concern in CHB-MLI is the Total Harmonic Distortion (THD) caused by the switching algorithm that is not optimized, which can cause harm to the systems due to low power quality and efficiency. This paper addresses the issue of THD in CHB-MLI by proposing a modified Carrier-Based Pulse Width Modulation (CB-PWM) technique, namely the Third Harmonic Injection Square Pulse Width Modulation (THI²-PWM). The proposed method also aims to improve DC bus utilization. To validate the effectiveness of the THI²-PWM technique, simulations were carried out using MATLAB Simulink for a 5-level CHB-MLI system. The results demonstrate improved performance compared to conventional CB-PWM methods.

Keywords

Carrier-Based PWM, Cascaded H-Bridge, Multilevel Inverter

1. Introduction

In modern power electronic systems, the demand for efficient power conversion with low losses is becoming increasingly important. Power electronic devices with high efficiency are more reliable and less likely to fail. One commonly used device is the multilevel inverters, which are essential in high-power applications such as

renewable energy systems, electric vehicles, industrial motor drives, and HVDC transmission. The CHB-MLI is widely used for medium and high-power needs because it can produce an output waveform close to a pure sine wave, helping to reduce harmonic distortion and electromagnetic interference [1]-[3]. However, one of the main challenges with CHB-MLI is reducing Total Harmonic Distortion (THD) to improve power quality. Harmonics can cause power loss, overheating, and lower efficiency, which affects the reliability and lifespan of electrical equipment [4] [5]. Although multilevel inverters generally have lower THD than two-level inverters due to their smoother waveforms, THD can still increase if the switching control is not optimal [6]. As the number of levels rises, switching becomes more complex and harder to manage. To solve this, several CBPWM methods like Phase-Shifted and Level-Shifted PWM have been developed to improve switching patterns and reduce THD [7] [8]. This project aims to evaluate the harmonic reduction and DC bus utilization of 5-level CHB-MLI by comparing conventional CBPWM techniques with a proposed THI^2 -PWM technique. The results are expected to highlight the improvement of the proposed THI^2 -PWM technique over conventional CB-PWM techniques in terms of output waveform quality.

2. Multilevel Inverter

2.1. Cascaded H-Bridge Multilevel Inverter

The Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is commonly used in medium- to high-power applications, including renewable energy systems and industrial motor drives [2] [3] [9]. It consists of multiple single-phase H-bridge power cells, which are typically connected in series on the AC side to generate a stepped output waveform that closely approximates a sinusoidal signal with reduced harmonic distortion [10]. **Figure 1** shows the circuit of 5-level CHB-MLI.

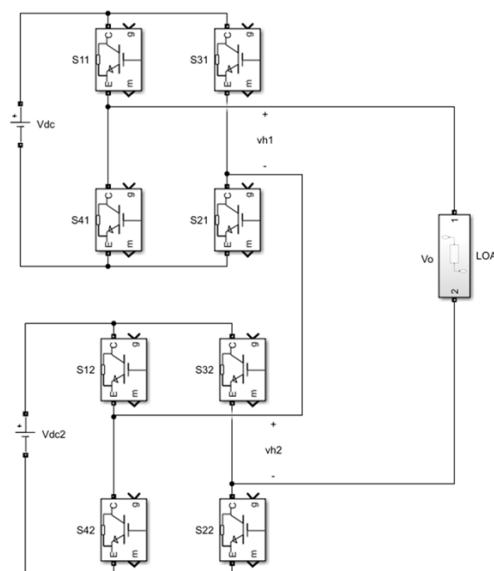


Figure 1. Circuit of 5-level CHB-MLI.

2.2. Total Harmonics Distortion

Harmonic distortion is a significant issue in electrical power systems, often leading to system disturbances and reduced power quality. The increasing use of power electronic devices, particularly converters and inverters, has contributed to higher levels of Total Harmonic Distortion (THD), which affects electrical power across a wide range of frequencies [11]. These distortions are primarily caused by non-linear loads within the system, where the current waveform deviates from the ideal sinusoidal shape typically seen in linear load conditions. Harmonics can be described as the presence of additional waveforms whose frequencies are integer multiples of the fundamental frequency [12]. The superposition of these harmonic components on the fundamental waveform results in signal distortion, as illustrated in **Figure 2**.

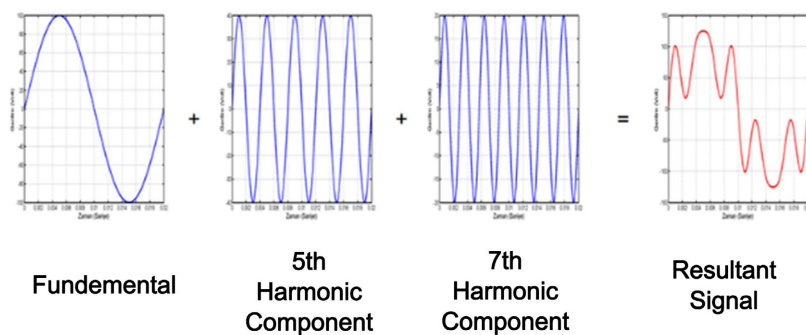


Figure 2. The representation of harmonics affecting fundamental signal.

2.3. DC Bus Utilization

In voltage-source inverters, DC bus utilization is defined as the ratio of the output fundamental voltage amplitude to the available DC link,

$$\eta_{\text{bus}} = V_{1,\text{peak}} / V_{dc,\text{available}} \quad (1)$$

where V_1 is the fundamental of the inverter output voltage, and $V_{dc,\text{available}}$ is the total DC link the topology can impress across the output without entering over-modulation. This parameter evaluates how effectively the inverter converts the available DC voltage into useful AC fundamental voltage. A higher fundamental voltage at the same DC link directly implies better utilization, as a larger portion of the DC bus is converted into usable output rather than being limited by the modulation process [13].

2.4. Carrier-Based PWM

Carrier-Based Pulse Width Modulation (CB-PWM) is a widely adopted technique for controlling the switching of power devices in multilevel inverters, particularly in Cascaded H-Bridge Multilevel Inverters (CHB-MLI) [7] [14]. The basic principle of CB-PWM involves comparing a modulation signal with one or more carrier signals to generate gate signals that control the ON and OFF states of the power switches. One of the key reasons CB-PWM remains popular is its simplicity of

implementation. Unlike Space Vector PWM (SV-PWM) and Model Predictive Control (MPC), CB-PWM is not computationally demanding and does not require high-performance microcontrollers. In addition, CB-PWM has been shown to be effective in reducing the Total Harmonic Distortion (THD) of the CHB-MLI output waveform [14] [15]. There are two main CB-PWM categories: Phase-Shifted PWM (PS-PWM) and Level-Shifted PWM (LS-PWM) [7] [8]. In PS-PWM, all carrier signals share the same peak amplitude and frequency but are phase-shifted relative to each other. The phase shift depends on the desired number of voltage levels and the inverter topology. **Figure 3** illustrates an example of PS-PWM applied to a 5-level CHB-MLI. On the other hand, in LS-PWM, each carrier signal also has the same peak and frequency, but they are vertically stacked on top of each other. LS-PWM includes three carrier arrangements: In-Phase Disposition PWM (IPD-PWM), where all carriers are in phase (shown in **Figure 4**); Alternate Phase Opposition Disposition PWM (APOD-PWM) where carriers are alternately in phase and out of phase (shown on **Figure 5**); and Phase Opposition Disposition PWM (POD-PWM), where carriers above the zero reference are in phase while those below are out of phase (shown in **Figure 6**). Each modulation technique has different implementation characteristics and produces different effects on the inverter's performance depending on the selected CB-PWM strategy.

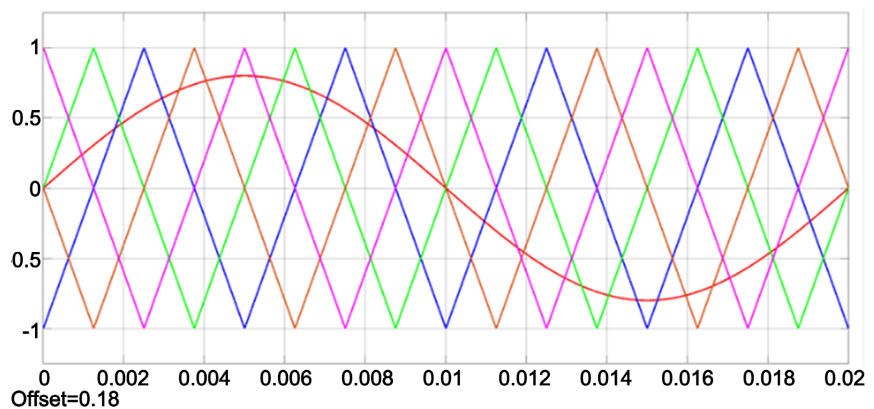


Figure 3. PS-PWM for 5-level CHB-MLI.

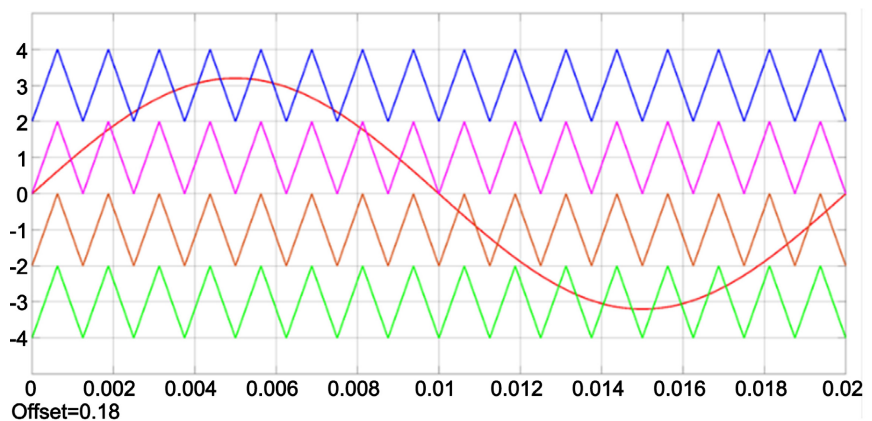


Figure 4. IPD-PWM for 5-level CHB-MLI.

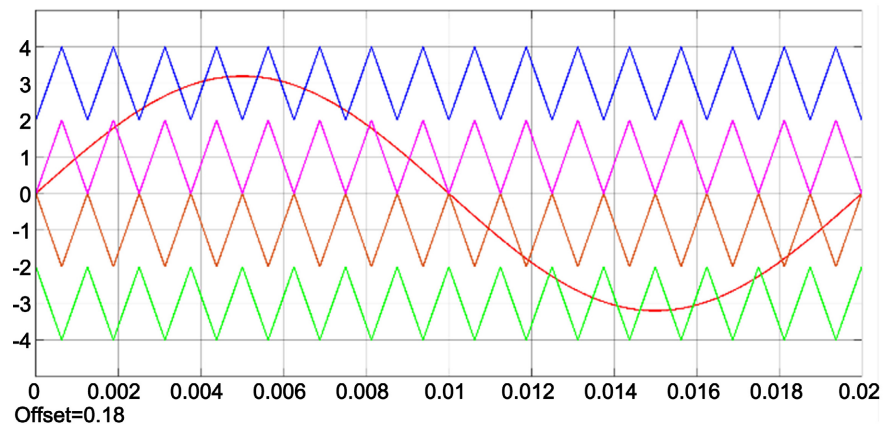


Figure 5. POD-PWM for 5-level CHB-MLI.

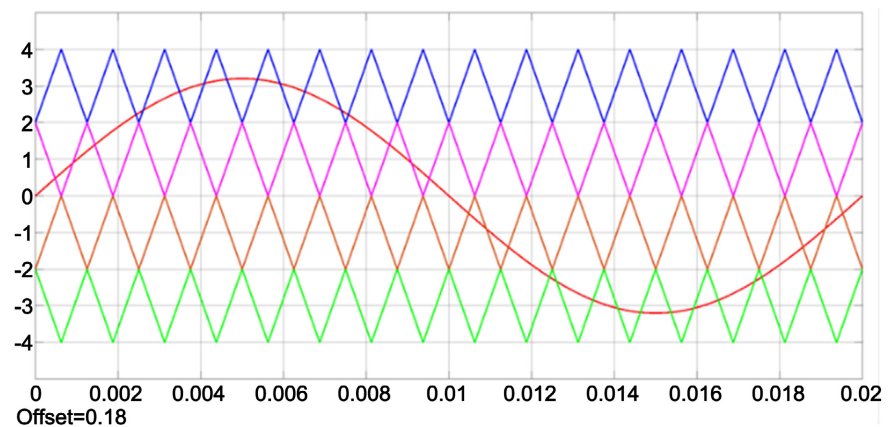


Figure 6. APOD-PWM for 5-level CHB-MLI.

2.5. Proposed Carrier-Based PWM

THI²-PWM is a unique method developed in [16] specifically for a 5-level three-phase Cascaded H-Bridge Multilevel Inverter (CHB-MLI) used in medium-voltage induction motor drive applications. The motivation behind the development of THI²-PWM was to address the issue of high torque ripple, which is a result of the pulsating torque introduced by conventional CB-PWM methods. The distinctive shape of the carrier signals used in this method can be observed in **Figure 7**. **Figure 8** illustrates the implementation of THI²-PWM in simulation, where the technique employs the Min function combined with Third Harmonic Injection (THI) to generate its unique carrier signal structure. Other advantages of the THI²-PWM method include lower output voltage THD, reduced stator current and voltage distortion, decreased power losses, smoother dynamic response in induction motor drives, and minimized torque ripple [16].

The THI²-PWM method presented in [16] was originally developed for three-phase CHB-MLI systems. In this project, when applied to a single-phase 5-level CHB-MLI, the output waveform exhibited a noticeable DC component, or DC offset, in the frequency spectrum, as shown in **Figure 9**, with the offset appearing at 0 Hz. In three-phase systems, the triplen (zero-sequence) content that accom-

panies third-harmonic injection cancels in the line-to-line voltages, so no net DC appears. In a single-phase topology there is no inter-phase cancellation path, and the injected zero-sequence biases the reference around the carrier, causes an imbalance between the positive and negative half cycles of the output waveform, as illustrated in **Figure 10**.

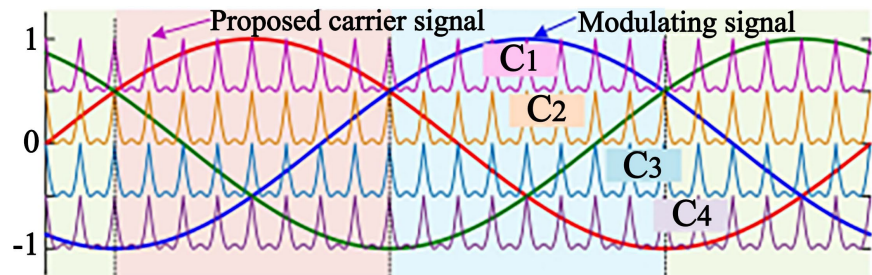


Figure 7. THI²-PWM for 3-phase 5-level CHB-MLI.

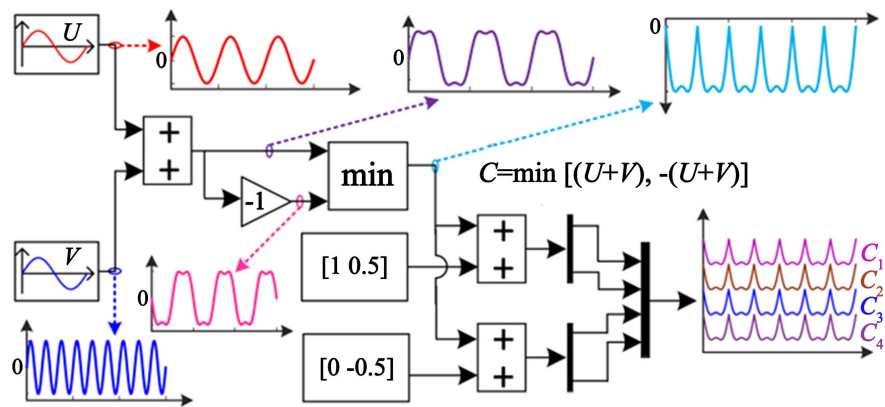


Figure 8. Implementation of THI²-PWM.

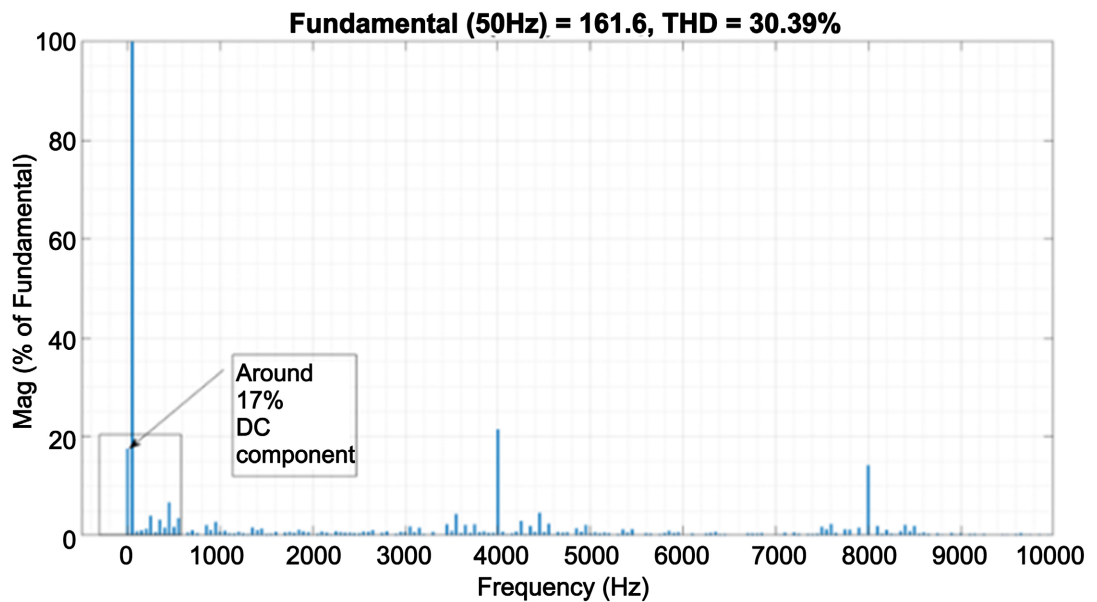


Figure 9. DC offset in frequency spectrum caused by THI²-PWM in single-phase CHB-MLI.

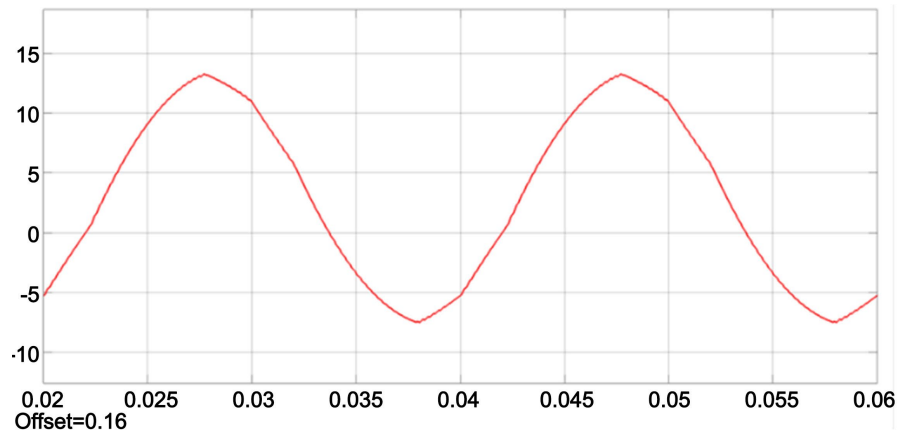


Figure 10. DC offset in frequency spectrum caused by THI²-PWM in single-phase CHB-MLI.

This DC bias is undesirable as it can cause DC current injection into the load or grid, violating standards such as IEC 61727 and IEEE 1547 [17]. To mitigate this, the proposed modified THI²-PWM generates a 180° phase-shifted twin of the injected reference and applies a Min-function with the lower carriers, ensuring symmetrical clipping and zero average voltage in each carrier period. This approach effectively removes the DC offset while maintaining the third-harmonic peak-flattening effect, thus preserving both the THD reduction and improved DC bus utilization.

3. Methodology

Implementation of THI²-PWM

The implementation of the THI²-PWM technique follows a similar procedure to LS-PWM, particularly in determining the carrier signal frequency and calculating the amplitude modulation index (M_a) for each CHB-MLI level. As a result, the carrier signal parameters used in THI²-PWM do not require separate calculation, since they share the same configuration as in conventional LS-PWM. The distinguishing feature of THI²-PWM lies in its use of third harmonic injection; a method commonly applied in three-phase inverters to enhance output voltage by modifying the reference signal with a third harmonic component at a specific amplitude. In THI²-PWM, however, the third harmonic is injected into the original carrier signal itself, generating the unique waveform required for the proposed modulation technique such as shown in **Figure 11**.

The injected signal can be represented as:

$$V_{cr} = 1.1547(2A_{cr})\sin\left(2\pi \times \frac{f_{cr}}{2}\right) + 0.19245(2A_{cr})\sin\left(2\pi \times \frac{3f_{cr}}{2}\right) \quad (2)$$

where:

A_{cr} = carrier signal amplitude

f_{cr} = carrier signal frequency

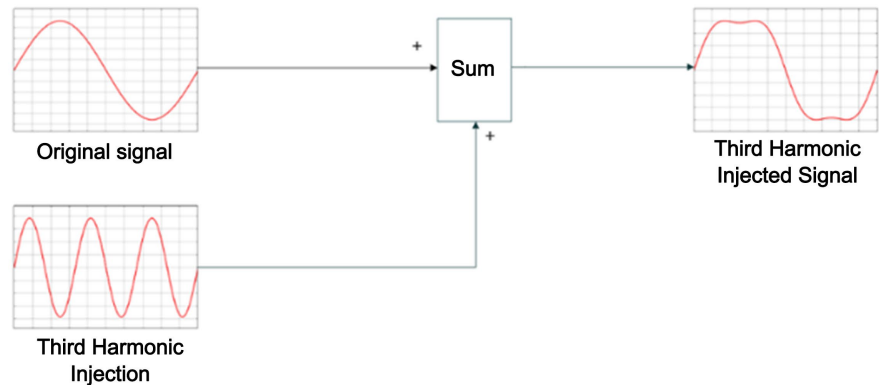


Figure 11. Third harmonic injection.

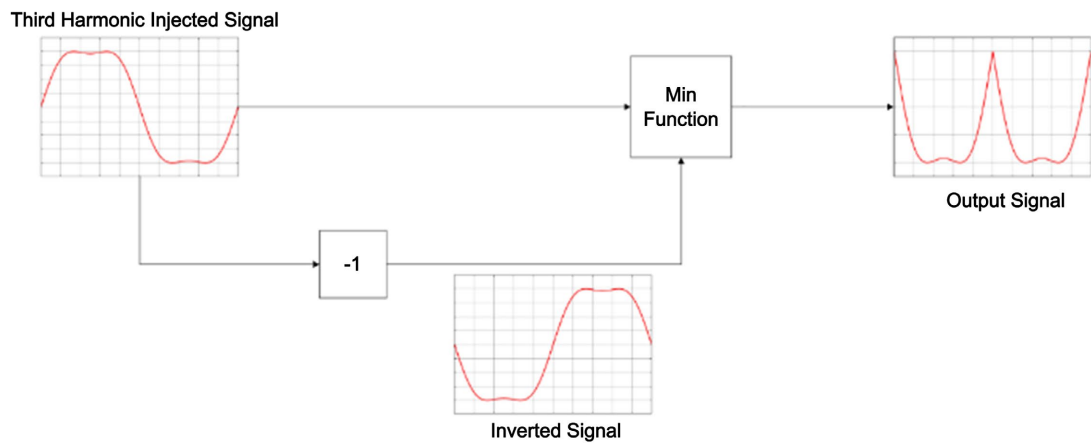


Figure 12. THI²-PWM carrier signal generation.

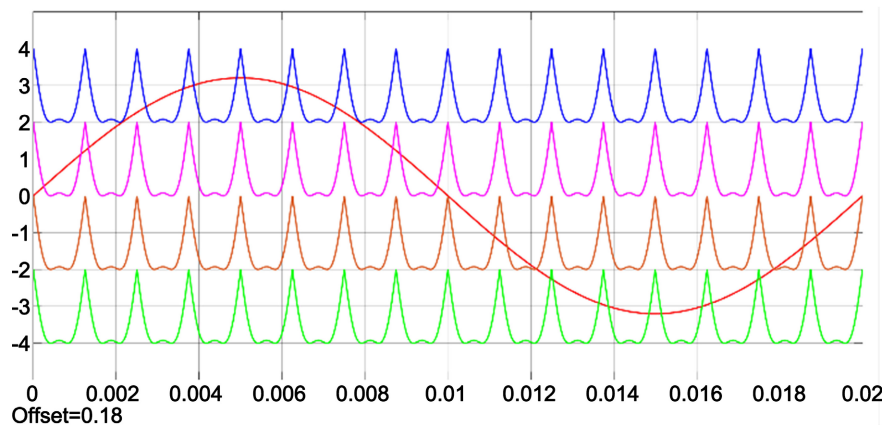


Figure 13. THI²-PWM for single-phase 5-level CHB-MLI.

After that, the third harmonic injected signal must be phase shifted by 180 degrees and compare it with initial signal using Min function to extract lowest value from both waveforms, such as shown in **Figure 12**. Whereas the arrangement of carrier signal for single-phase 5-level CHB-MLI is as shown in **Figure 13**. Since the original technique injects DC offset into the load, the carrier signals must be modified by changing the arrangement of the bottom two carrier signals, such as

shown in **Figure 14**. The overall block diagram for the modified THI²-PWM method is as shown in **Figure 15**.

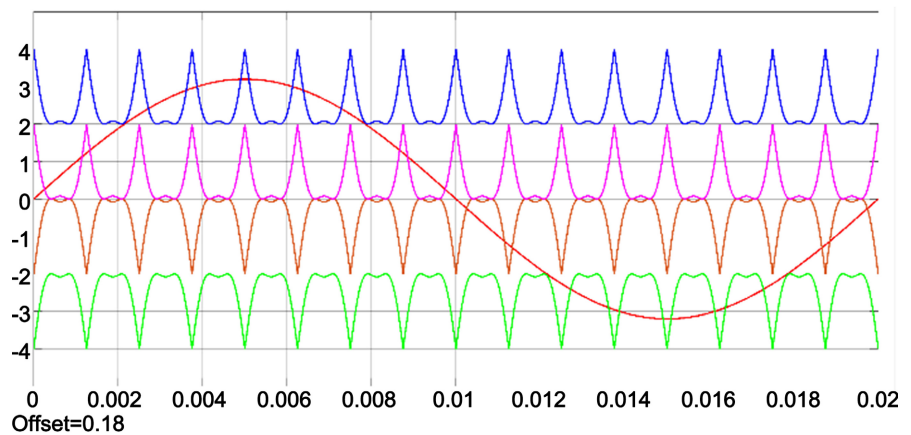


Figure 14. Modified THI²-PWM.

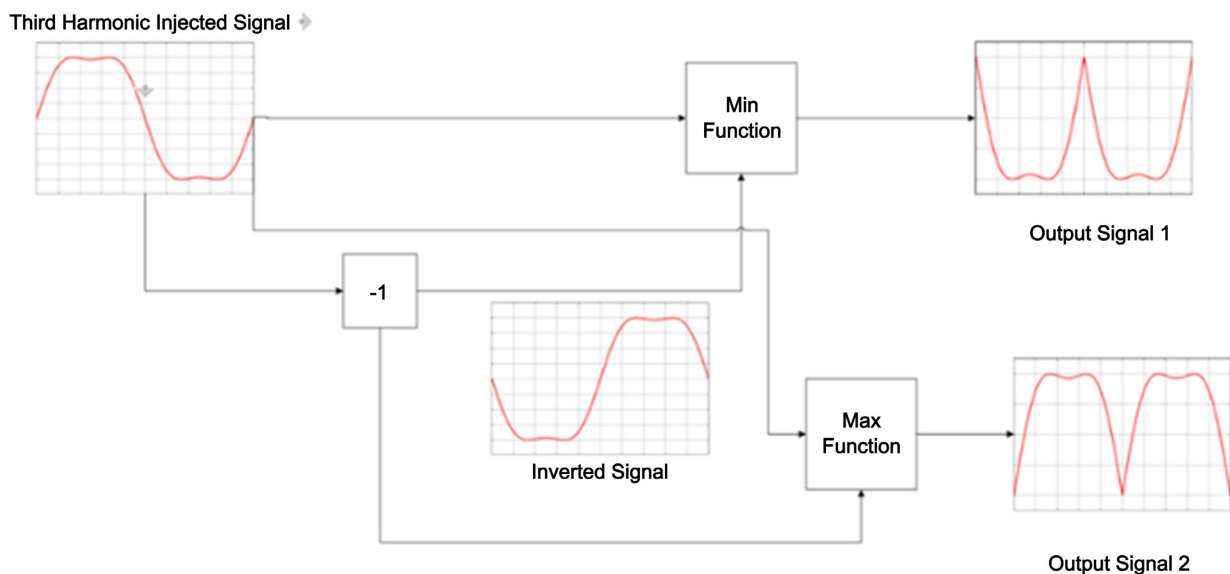


Figure 15. Modified THI²-PWM implementation.

MATLAB Simulink simulations of single phase 5-level CHB-MLI using conventional CB-PWM and modified THI²-PWM methods are conducted as shown in **Figure 16**. In the simulation, the total DC supply voltage combined from all H-Bridge cells is 200 V, the load consists of a 10 Ω resistor and a 40 mH inductor, and the output voltage operates at a frequency of 50 Hz and switching frequency of 4 kHz. The switching frequency of 4 kHz was selected as a practical compromise between harmonic performance and switching losses, giving an f_{sw}/f_1 ratio of 80 (4 kHz/50 Hz), which is well above the minimum recommended for carrier-based PWM to suppress low-order harmonics while limiting device stress. The total DC link voltage of 200 V was chosen as a safe, laboratory-scale value that ensures realistic device ratings and load sizing without affecting percentage THD, since in

the linear modulation region the harmonic spectrum scales proportionally with voltage. The relative THD improvement achieved by the proposed modified THI²-PWM over conventional CB-PWM methods is expected to persist for higher switching frequencies or different DC link voltages, as it originates from the modulation strategy itself rather than the specific operating point.

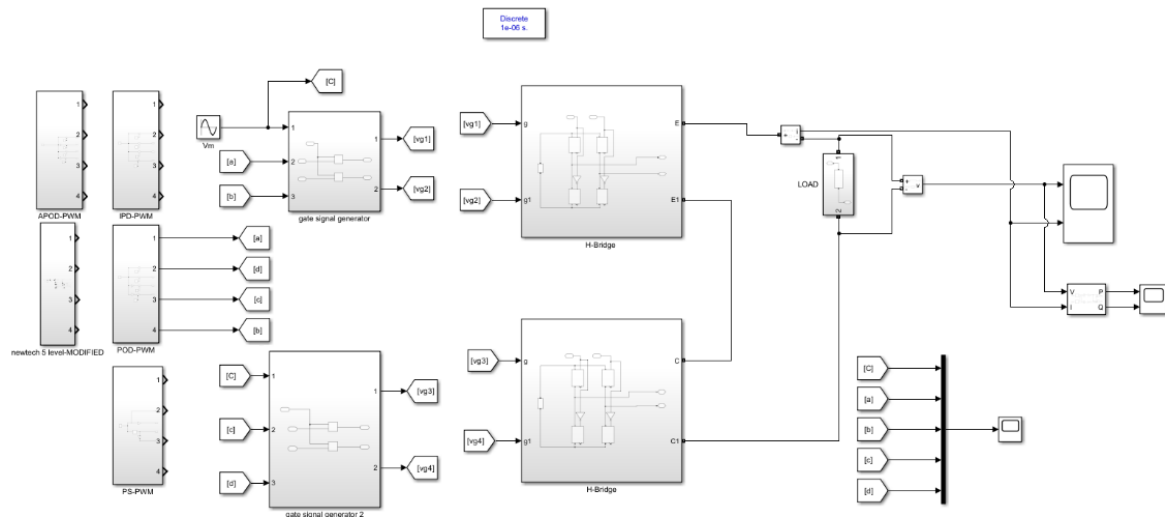


Figure 16. MATLAB Simulink implementation of 5-level CHB-MLI.

4. Results

The output voltage of the 5-level CHB-MLI was measured and recorded using the Scope block and FFT Analyzer. As shown in **Figure 17**, the waveform represents the output voltage of a 5-level CHB-MLI. The CHB-MLI topology produces a five-step output voltage waveform, which corresponds to the number of voltage levels defined by the inverter configuration.

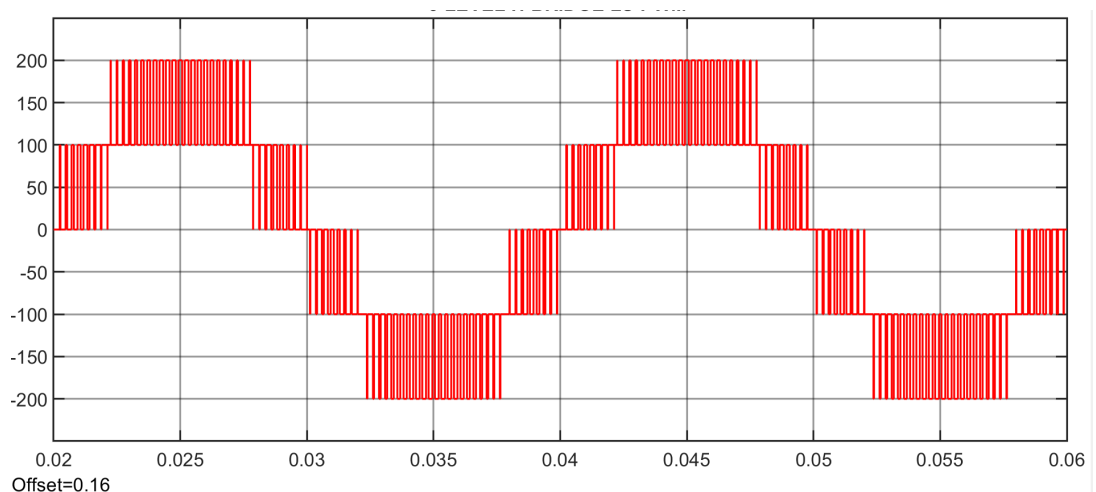


Figure 17. Output voltage of 5-level single-phase CHB-MLI.

The frequency spectrum of voltage THD of 5-level CHB-MLI (for $M_a = 0.8$)

with conventional CB-PWM methods are shown in **Figure 18** (PS-PWM), **Figure 19** (IPD-PWM), **Figure 20** (APOD-PWM), **Figure 21** (POD-PWM) while **Figure 22** shows frequency spectrum of modified THI^2 -PWM method. **Table 1** summarizes the voltage THDs of all these methods whereas compared to conventional CB-PWM methods, THI^2 -PWM achieves the lowest THD at 28.21%, representing around 5% improvement over the conventional CB-PWM methods. This enhancement is attributed to the spread-out nature of harmonic components and the strategic injection of a third harmonic into the carrier signal, effectively suppressing dominant low-order harmonics.

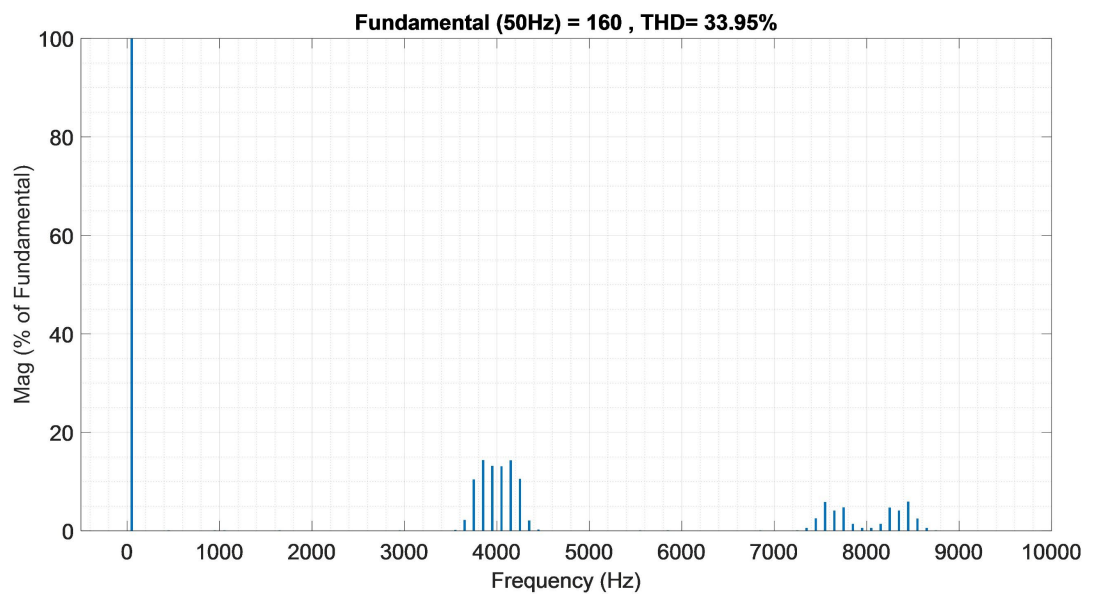


Figure 18. Frequency spectrum of 5-level CHB-MLI for PS-PWM.

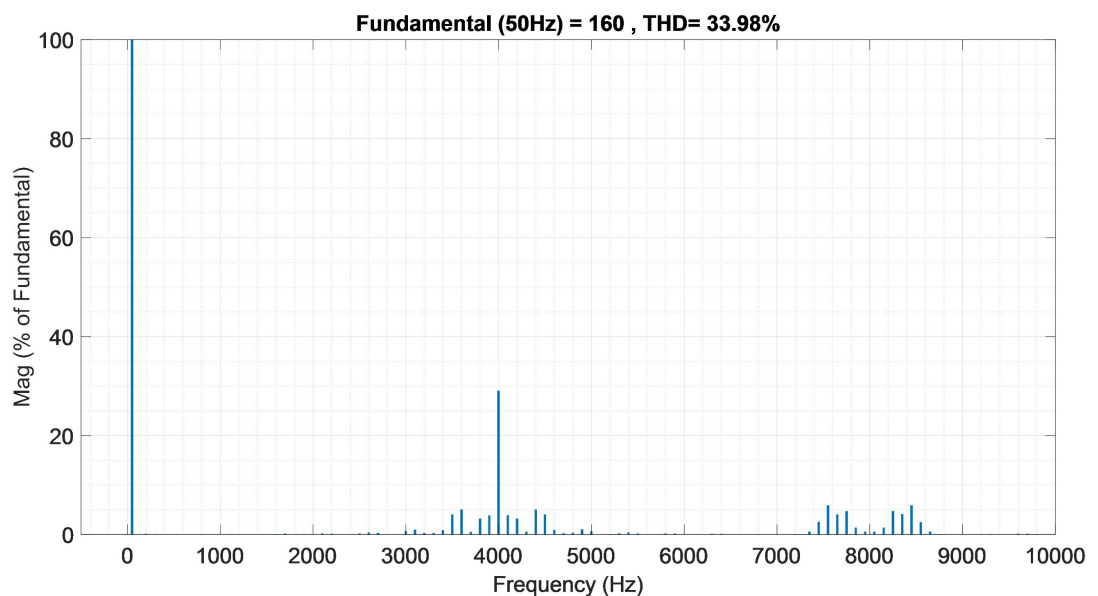


Figure 19. Frequency spectrum of 5-level CHB-MLI for IPD-PWM.

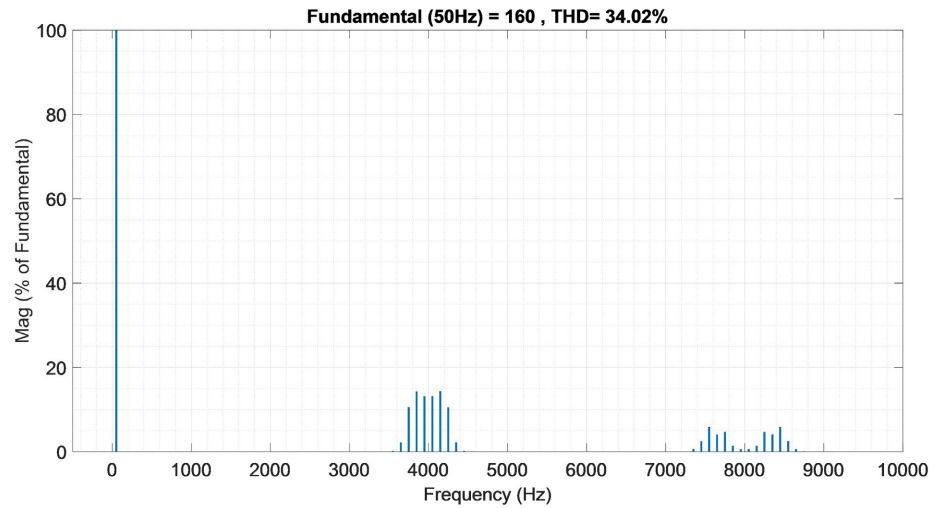


Figure 20. Frequency spectrum of 5-level CHB-MLI for APOD-PWM.

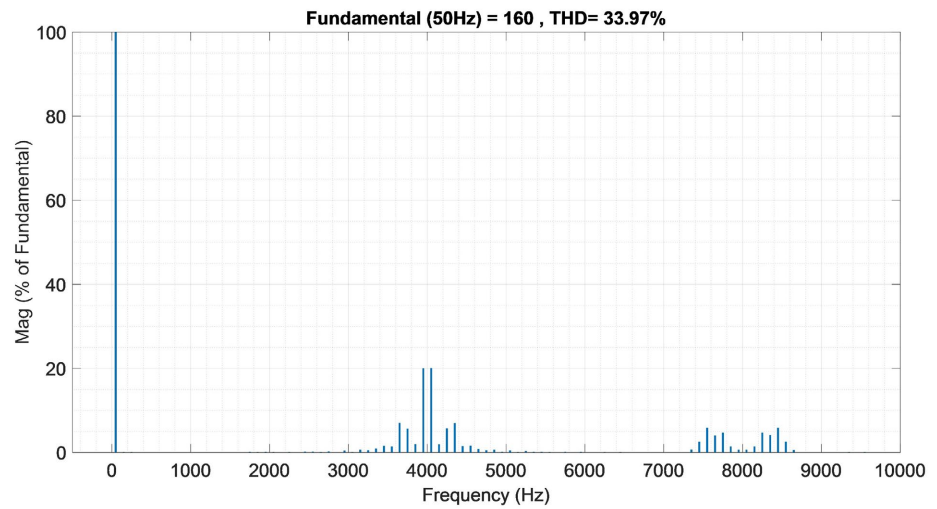


Figure 21. Frequency spectrum of 5-level CHB-MLI for POD-PWM.

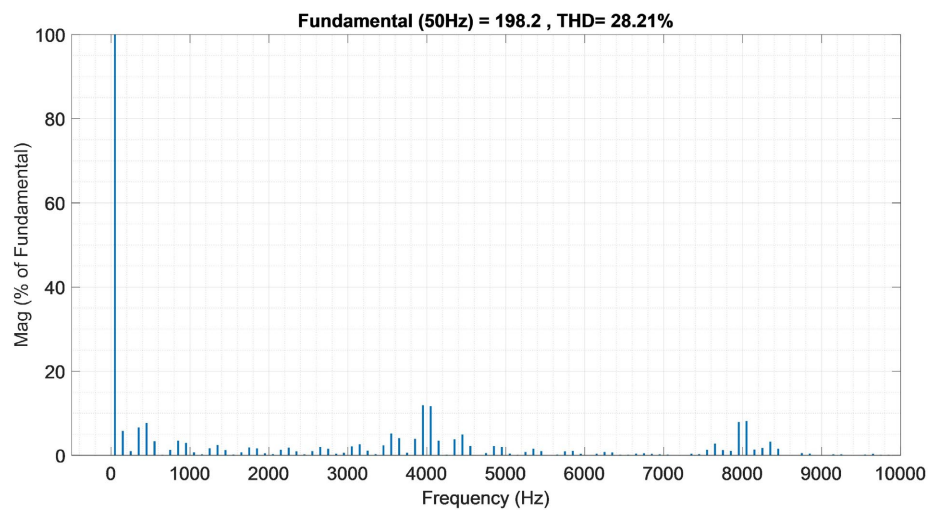


Figure 22. Frequency spectrum for modified THI^2 -PWM.

Table 1. Output voltage THD at amplitude modulation index, $M_a = 0.8$.

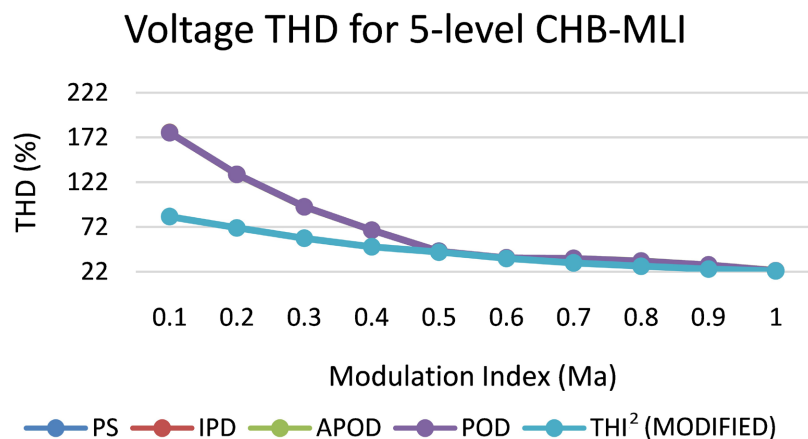
Modulation method	PS-PWM	IPD-PWM	APOD-PWM	POD-PWM	THI ² -PWM (Modified)
Voltage THD	33.95%	33.98%	34.02%	33.97%	28.21%

In addition to the observed reduction in output voltage THD, the modified THI²-PWM technique also showed enhanced DC bus utilization as tabulated in **Table 2**. In the presented results, for the same 200 V DC bus, the conventional CB-PWM methods produces a fundamental of 160 V, whereas the proposed modified THI²-PWM achieves 198.2 V, a 24% increase, thereby indicating a proportional improvement in DC bus utilization. This improvement stems from effect of third-harmonic injection, which flattens the reference waveform peaks and extends the linear modulation range, enabling a higher fundamental voltage before over-modulation occurs. This aligns with theoretical findings in [7] [13] [16], where harmonic injection methods have been shown to enhance inverter performance and reduce distortion without increasing switching complexity.

Table 2. Comparison of fundamental voltage amplitude for each CB-PWM technique.

Modulation method	PS-PWM	IPD-PWM	APOD-PWM	POD_PWM	THI ² -PWM (Modified)
Fundamental voltage amplitude	160 V	160 V	160 V	160 V	198.2 V

To complete the analysis, simulation was also conducted for all CB-PWM method for the linear range of modulation index and its results are tabulated in **Figure 23**. It can be observed that the modified THI²-PWM maintains better performance across a range of modulation indices, further validating its robustness. These results confirm the method's potential for high-performance applications requiring both low THD and high efficiency, such as in renewable energy and motor drive systems.

**Figure 23.** 5-level CHB-MLI with CB-PWM comparison for output voltage THD.

5. Conclusion

This study introduced a modified CB-PWM technique, referred as THI²-PWM, aimed at reducing output voltage THD and improving DC bus utilization in a 5-level CHB-MLI. The uniqueness of this method lies in its use of third harmonic injection directly into the carrier signal, enhanced by a signal-clipping Min function, which differentiates it from traditional third harmonic modulation strategies. The technique was implemented in MATLAB Simulink by injecting a third harmonic component into the carrier waveform and shaping it using signal clipping logic. Simulation results validate the superiority of the modified THI²-PWM over conventional methods (PS-PWM, IPD-PWM, APOD-PWM, POD-PWM), with a significant THD reduction to 28.21% and a 24% increase in fundamental voltage amplitude. These findings affirm theoretical claims that harmonic injection and optimized carrier arrangements can lead to better waveform quality and improved energy conversion efficiency while avoiding the complexity of advanced modulation schemes such as Space Vector PWM (SVPWM).

This study focuses on the conceptual development and numerical evaluation of the modified THI²-PWM technique for single-phase cascaded H-bridge multilevel inverters. At this stage, detailed MATLAB/Simulink modeling was used to enable controlled, repeatable comparisons between multiple carrier-based PWM methods under identical operating conditions, which is often not feasible in early experimental setups due to hardware and measurement constraints. The simulation environment incorporates device-level switching behavior, carrier synchronization, and harmonic analysis consistent with established PWM modeling practices reported in literature, allowing for accurate prediction of spectral performance and DC bus utilization trends.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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