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Electrothermal Modelling Methodology of SiC Power MOSFET for Evaluation of Failure Cases during Short-Circuit Phases

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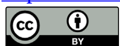
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Abstract

We present the complete methodology to propose an efficient electrothermal model of the Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET), largely used in high-power operations. The detailed model describes the non-linear electro-thermal dependencies of influent parameters in this device, such as transconductance (g_m), on-state resistance (R_{DSON}), threshold voltage (V_{GSTH}) and parasitic capacitive elements. The rigorous identification of their values for implementation into the model is based on initial empirical and experimental determinations, which are finely processed and optimized by genetic algorithm methods (NSGA). This model is combined with a Cauer's thermal network, determined at the chip package level, to perform electrical simulations of the SiC MOSFET activity, including the temperature couplings. With comparisons of experimental and calculated features of the MOSFET chip, validations of the model have been proved both for normal activity and for the outside range of operations of the device. Because of actual challenging issues of the reliability of SiC power transistors, electrothermal models and simulations can help to prevent effects of failure cases such as short-circuit events and assist in the diagnostic monitoring of these devices under high power and switching conditions.

Keywords

Cauer Network, Electrothermal Model, Genetic Algorithm, Junction Temperature, MOSFET, Power Circuit, Silicon Carbide (SiC), Short-Circuit, Threshold Voltage, Transconductance

1. Introduction

The technological readiness of the Silicon Carbide (SiC) Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) dedicates theirs for improved power electronics features [1] [2], and these components are nowadays widely used in actual converters for high-performance electrical applications [3]-[5]. This is the case for actual electrical motorization and railway traction chains, where the power converter is an essential feature. For this reason, this technology is constantly challenged in terms of robustness, given the demands for performance and reliability [6]. As power MOSFET with SiC semiconductors can achieve both high voltage, elevated temperature and high frequency operations [7], the electrothermal activity is inherently enhanced and can degrade on-life reliability and ageing of the power chips and their physical environment and packaging materials [8] [9]. As a real improvement in energy efficiency (60%) in power converters, the major weakness of this actual emerging technology, which delays its global industrial deployment, is its reliability lifetime. Compared to Si IGBT (Silicon Insulated Gate Bipolar Transistor), chip manufacturer guarantees the nominal use of SiC MOSFET with only one single Short-Circuit (SC) event of 1.2 μs of maximum duration, as it tolerates 100 SC events of 10 μs each for IGBT transistors. Consequently, in converters used in railway traction, for example, surveys of the default operations as short-circuit, delamination of chip area and bonding pull-out become critical and new challenges at the earliest design phase to prevent and avoid destruction of the electronics [10] [11]. In the literature, several papers show the importance of the thermal aspects on SiC MOSFET electrical features, and some ways to analyze, model and simulate these electro-thermal characteristics [12]-[14]. Authors have proposed some models well adapted to SiC components derived from anterior physics-based Silicon MOSFET technology [15]-[17]. This approach requires detailed knowledge of fabrication and technology of the device, issued by the manufacturer, and some simplified assumptions regarding the real complexity of semiconductor technology.

Simulations using these analytical models can efficiently reproduce rigorously nominal and specific operational conditions of the device, but are dependent on a high level of semiconductor and physical parameter extraction and implementation. An alternative is to develop behavioral modelling techniques to complete or replace the electrical equivalent circuit components, particularly considering their package passive components and cabling [18]. We can also conduct multiple parametric simulations during the prototyping and design process, incorporating external physical effects such as temperature. The parameter values for this modelling are user-defined, based on individual characterizations, and supplemented by external information provided by manufacturers. The following drawbacks must be considered. First, there is a challenge in defining and obtaining a relevant set of measurements from the device at external terminals, which depend on specific and limited operating points. Additionally, the numerical post-processing involves fitting procedures on the set of parameters, which must retain maximum

physical significance.

To simulate the electrothermal couplings involved in this technology, it is essential to conduct a thorough and rigorous investigation into the relationships between electrical and thermal physics in wide bandgap transistors. References [12]-[18] highlight all the major difficulties and key issues, especially for devices based on WBG semiconductors, SiC and GaN (Gallium nitride): the physical phenomena are not governed by the same time constants, with electrical phenomena occurring in the order of nanoseconds, while thermal phenomena often occur on the order of seconds.

This paper proposes to comply with these challenging issues, by describing mixed analytical, numerical and experimental steps and methods to develop a robust electrothermal model for SiC MOSFET devices, enhancing their efficiency in realistic and predictive simulations. In the first section, the thermal-electrical model developed for SiC MOSFET transistor is presented. We describe the thermal and non-linear dependency of the drain-source resistor, the threshold voltage, and the transconductance in a generic SiC MOSFET model. In the second section, we present our methods to optimize and implement the parameters and the coefficient of this model. We apply these calculations to an industrial SiC MOSFET in TO-247 package, and perform identifications using a specific optimization procedure, the genetic algorithm, which remains valid across all operating ranges of the devices and overall. Then, in the last section, results of electrothermal simulations are compared to thermal-electrical experimental curves of the chip, to appreciate the range of validity and the quality of the modelling approach. For final use, we propose a simulation procedure for extreme cases of power component activity, such as short circuit events, with high variations of current and temperature. We conclude on the robustness of this short-circuit simulation of power modules, and its interest and application in the Reverse Biased Safe Operating Area (RBSOA) to help and pre-validate the design test. These results also validate the first main step of realistic electrothermal models at the semiconductor and single-discrete chip level with SiC technology, necessary to extend the method to more complex power modules and packs with high-level features for electrical traction in trains.

2. Electro-Thermal Model of a SiC MOSFET Transistor

2.1. Topology of the SiC MOSFET Model

The generic electrical model of MOSFET transistors has been now well established with different calculations and equations based on physical semiconductor properties and dimensional topology of the chip [19]-[21]. The fundamental principle of a MOSFET device, as Field-Effect-Transistor (FET) family, is the capability to modulate the output current at the drain $I_{Drain\text{-}Source}$ among the control voltage at the input $V_{Gate\text{-}Source}$. Continuous works have been driven for refining these equations of the output characteristics among the different improvements and realizations of multiple type of MOSFET and their applications [22] [23]. For power MOSFET, that is constructed with vertical conduction in the semi-conductor lay-

ers for optimization of power switching operations, the analytical model of the drain current I_{DS} with external electrical conditions of operations (V_{GS}, V_{DS}) is resumed by the following equations for the ON/OFF modes:

For $V_{GS} < V_{TH}$: cutoff mode, then $I_{DS}(V_{GS}, V_{DS}) \approx 0$

For $V_{GS} > V_{TH}$: conduction mode, then $I_{DS}(t) = f[V_{GS}(t), V_{DS}(t)]$

for $V_{DS} < V_{DSSAT} = (V_{GS} - V_{TH})$, then $I_{DS}(V_{GS}, V_{DS}) \approx K^* V_{DS}$: linear or ohmic mode

for $V_{DS} > V_{DSSAT} = (V_{GS} - V_{TH})$, then $I_{DS}(V_{GS}, V_{DS}) \approx I_{DS}(V_{GS})$: saturated mode, the current I_{DS} is independent of the variation and the increase of V_{DS}.

Another representation of I_{DS} variation is to consider the equivalent gain denoted g_m (transconductance), that represents the ratio (derivative) of drain current I_{DS} generated by the voltage V_{GS} applied on the gate, at a fixed value of output voltage V_{DS}:

$$g_m = \left. \frac{\delta I_{DS}}{\delta V_{GS}} \right|_{V_{DS} = constant} \tag{1}$$

This is a more convenient approach for electrical modelling of the output features of MOSFET, because it implies only an equivalent current source with single voltage control (V_{GS}). For Power chips in switching use with only two states of electrical output conditions, transconductance gm, at a functional value of $V_{DS} > V_{DSSAT} = (V_{GS} - V_{TH})$ stays quite constant in conduction mode, and I_{DS} vary linearly with V_{GS} (**Figure 1**).

$$I_{DS} = g_m \cdot V_{GS(V_{DS} = constant)} \tag{2}$$

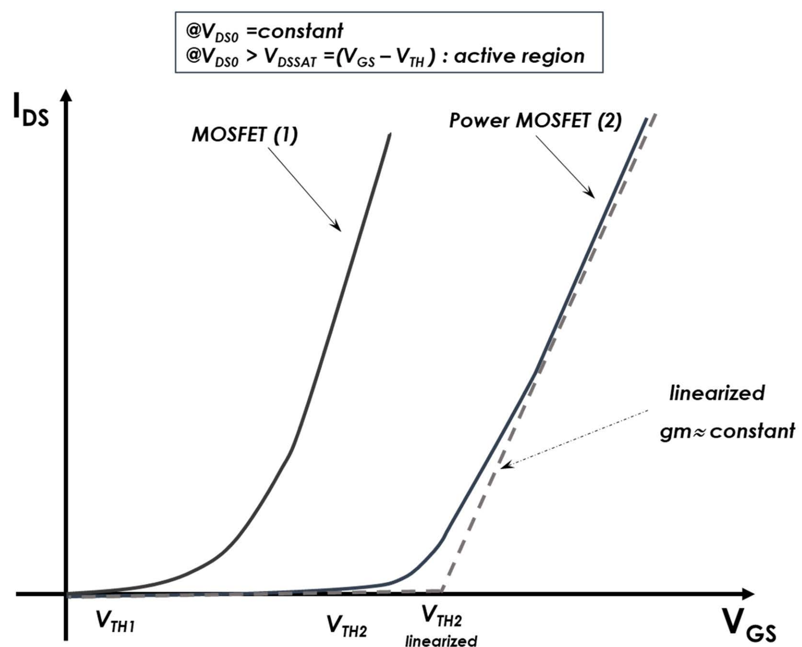

Figure 1. Ideal transfer characteristics $I_D(V_{GS})@V_{DS}$ = constant and transconductance gm of MOSFET transistors. 1-Digital MOSFET (horizontal conduction); 2-Power MOSFET (vertical conduction).

In a second step, for access to realistic representation of static and dynamic responses of the MOSFET cell, the model is completed with resistive and capacitive equivalent effects, deduced from physical topology of the semiconductor layers and materials [23] [24]. Firstly, the different conductive losses can be identified by the intrinsic resistances naturally implemented or activated in the conductive and semiconductor layers (**Figure 2**) with current paths.

$$R_{DS} = R_{n+} + R_{CH} + R_A + R_J + R_D + R_{SB} \tag{3}$$

with:

R_{n+}: diffusion source resistance of the n^+ region, very low contribution to the total value of $R_{DS(ON)}$.

R_{CH}: channel resistance, vary with geometry of the channel during operations.

R_A: accumulation resistance. When $V_{GS} > 0$, electric charges accumulate in the n^- region near the gate area.

R_J: component resistance in the n^+ region between the two p-body regions.

R_D: drift region resistance, localized in the main n^- region, under the two p-body regions to the n^+ substrate region(drain). Main contribution to the global $R_{DS(ON)}$ at high V_{DS}.

R_{SB}: substrate resistance, important at lower voltages (<50 V).

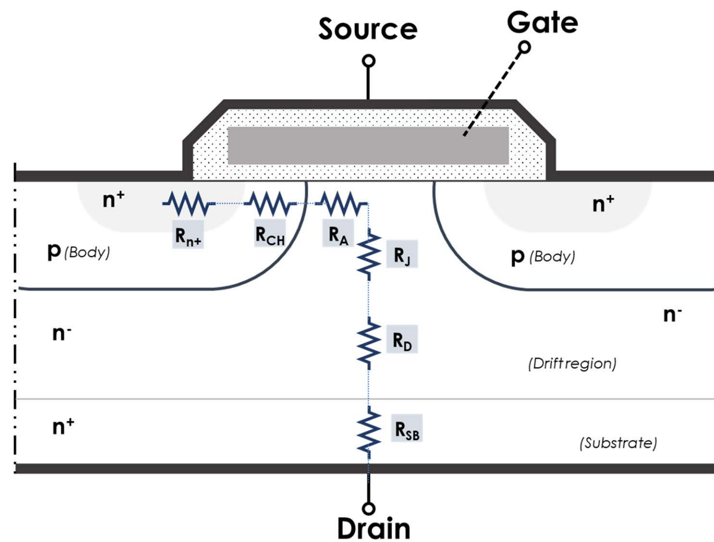

Figure 2. Origin of internal resistances of the n-channel power MOSFET in ON-state operation.

For Power MOSFET model, at the ON-state of the chip, when current in the drain is consequent, we consider that the global resistance R_{DSON} is mainly represented by the contributions of the drain resistance R_D, and the N-layer resistance R_a.

$$R_{DSON} = R_A + R_D \tag{4}$$

Secondly, intrinsic capacitive effects (**Figure 3**) can be defined with the topology and the placement of the conductive materials (doped layers, metallic termi-

nals) and dielectric ones (SiO_2). Two of these capacitors, C_{GS} between gate and source, and C_{GD} between gate and drain, can be directly extracted from the geometry of the device. Capacitance C_{GS} is formed by the overlap of the source and the channel regions recovered by the gate electrode. Its definition and value depend mainly on the dimensions and geometry of the regions, and can be considered as the contributions of the 3 intrinsic capacitances C_{n+}, C_O and C_p all in a parallel disposition:

$$C_{GS} = C_{n+} + C_O + C_p \tag{5}$$

$$C_{GD} = \frac{C_{GD,0}}{1 + K_1 \cdot \sqrt{V_{DS}}} \tag{6}$$

with: $C_{GD,0}$ initial value of C_{GD} ($V_{DS} = 0$).

K_1 fitting parameter.

Fundamentally, C_{GS} and C_{GD} are affected by depletion layers within the voltage across them during device operation. But it is observed that C_{GS} only has very small change, compared to C_{GD}, so it can be assumed as invariable under different electrical operating conditions.

The third capacitance is the one considered between drain and source, C_{DS}. It corresponds to a normal defined junction capacitance of the parasitic body diode, inherent to the structure of vertical MOSFET. Its equation shows also non-linear behavior among the voltage V_{DS}:

$$C_{DS} = \frac{C_{DS,0}}{K_2 \cdot \sqrt{V_{DS}}} \tag{7}$$

with: $C_{DS,0}$ initial value of C_{DS} ($V_{DS} = 0$).

K_2 fitting parameter.

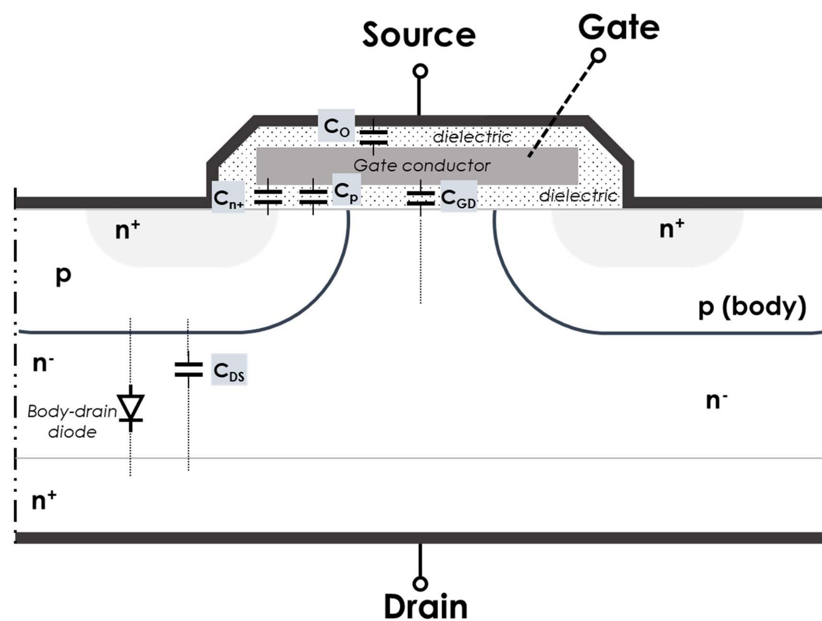

Figure 3. Origin of dynamic internal elements of the n-channel power MOSFET.

In modelling ways for power MOSFET, because threshold voltage V_{TH}, ON-state resistor R_{DSON} and transconductance gm are the main critical parameters for fine detailed representation of non-linear electrical and thermal dependencies of the global chip [25].

With these considerations and the description of these elements, an overall equivalent electrical model of the power MOSFET structure can be proposed, as illustrated in **Figure 4**. It is composed of the following components:

- A voltage-controlled current source $I_{DS} = f(V_{GS})$, with transconductance g_m (A/V) that is denoted.
- One resistor R_{DSON} (Ω) for losses representation at ON-State transistor.
- A fixed voltage source V_{GSTH} (V) in serial with an ideal diode, that represents the loss of voltage equivalent to the threshold voltage V_{TH} when transistor has stepped the conduction mode.

Other components included are the following:

- A diode D_{DS} representing the "body" diode, a p-n junction intrinsic to the overlap of p-n-p regions and layers of the structure of the power MOSFET (transversal).
- The three global capacitors, C_{GS}, C_{DS} et C_{GD}, to account for parasitic and time charge effects.

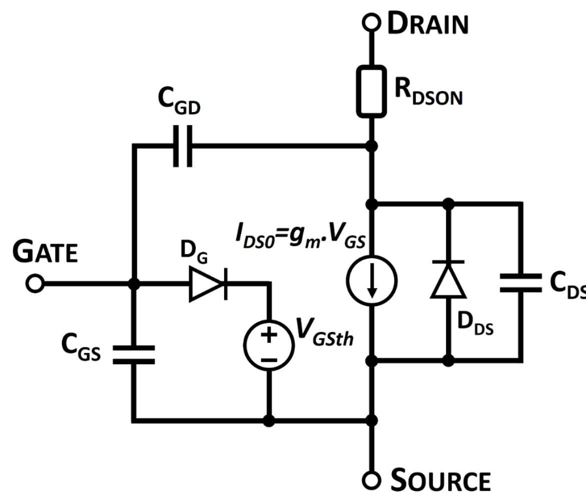

Figure 4. Topology of the proposed circuit model for SiC MOSFET chip.

All these parameters could be determined either by semiconductor physical parameters, if available, or by dedicated external characterization, given by the datasheet of the manufacturers, and/or by the user characterization. As many datasheets dedicated to power chips are consistent and well established for normal operations of a wide range of commercial power MOSFET, we will consider here the limits of some features that have to be finely simulated and anticipated. We focus especially on recent SiC devices that show new critical cases of operation in certain high-level applications, such as the electrical supply for trains and railways. From this point of view, considering the non-linear and temperature dependence of the

components of the electrical model is the key to this objective [26] [27]. The next step consists of defining the temperature dependency and feedback into nonlinear equations of some critical parameters and elements, such as R_{DSON}, g_m and V_{GSTH}.

2.2. Non-Linear Thermal Dependent Equations of SiC MOSFET

The parameters of the equivalent circuit are described by equations to recreate the linear, nonlinear, and thermally dependent features. For our purpose, these non-linear variations are critical because of their high sensitivity in electrical and thermal responses of the calculated electrical quantities, representatives of the reality of SiC MOSFET (*i.e.* high dV/dt, dI/dt, and dT/dt). For identifying correctly these parameters, analytical and optimization methods will be introduced after the description of the equations.

Firstly, the equivalent element R_{DSON}, which represents the drain-source resistance used to simulate on-state resistance, exhibits a linear behavior as described in the following equations [28].

$$R_{DSON}(T) = \alpha_1(T) \cdot I_D + \beta_1(T) \tag{8}$$

where $\alpha_1(T)$ is the temperature dependent coefficient for drain current I_D, and $\beta_1(T)$, is the initial temperature dependent coefficient for R_{DSON}. T is the temperature in Celsius degrees.

Equations of variations of $\alpha_1(T)$ and $\beta_1(T)$ are given at the second order of temperature, by the following expressions:

$$\alpha_1(T) = \lambda_1 \cdot T + \delta_1 \cdot T^2 + \psi_1 \tag{9}$$

$$\beta_1(T) = \lambda_2 \cdot T + \delta_2 \cdot T^2 + \psi_2 \tag{10}$$

with the R_{DSON} temperature factors: ψ_1, ψ_2 initial values; λ_1, λ_2 1st order values; δ_1, δ_2 second order values.

Several parameters are intrinsically linked to the threshold voltage V_{GSTH}. So, it is important to precisely understand the thermal dependence of V_{GSTH} to reproduce it rigorously. We use the following equation for $V_{GSTH}(T)$ with a calculation proposed for the description at the second order with the temperature [22] [24]:

$$V_{GSTH}(T) = \beta_2 + \varphi_1 \cdot T + \omega_1 \cdot T^2 \tag{11}$$

with the V_{GSTH} temperature coefficients: β_2, φ_1 and ω_1.

Transconductance gm, which represents the variation of the drain current I_D among the gate voltage V_{GS}, is a crucial parameter in MOSFET models. It exhibits complex non-linearity evolution that depends on the voltage output V_{DS}. For switching modes of power MOSFET, the ON-state operation of the transistor is forced in the active region with a value of $V_{DS} = V_{DS0} \gg (V_{GS} - V_{GSTH})$. Then, the typical curve $I_D = f(V_{GS})_{@V_{DS0}}$, denoted the output transfer characteristic, presents same non-linear variations in its slope, image of the transconductance g_m. We can usually observe and analyze three distinct regions (**Figure 5**) corresponding to the different inflexions of the slope (*i.e.* g_m). First initial region, for $V_{GS} < V_{GSTH}$, is the low-current source activity, with a flat low-level variation of I_D among

V_{GS}. Second region, with $V_{GS} > V_{GSTH}$, shows a quasi-linear rise of current I_D with V_{GS}. In this region, as V_{GS} still arises, we have the controlled-current source effect of the transistor. The last region is the saturation one, starting with $V_{GS} \gg V_{GSTH}$, where I_D becomes quite constant, at a maximum value denoted I_{DSS}.

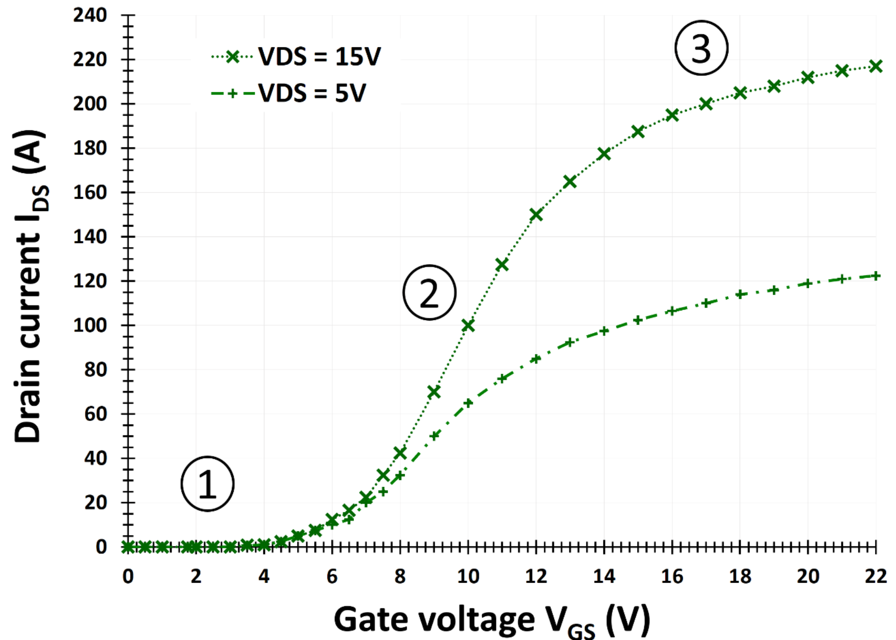

Figure 5. General variation of drain current as a function of gate voltage in MOSFET semiconductor with the three regions for two drain-source voltages(5 V; 15 V): 1—OFF region, 2—Current controlled source region 3—ON region.

In mathematics, the sigmoidal function presents a very similar shape with this output transfer characteristics of power MOSFET and the three non-linear regions. The sigmoidal function is analytically denoted $\sigma(x)$, where x is an argument in the real domain. Its representation is generalized with additional coefficients denoted k, A, and r, used for parametric adjustments of a family of curves:

$$\sigma(x) = \frac{k}{1 + A\mathrm{e}^{-r \cdot x}} \tag{12}$$

Numerical values of k, A and r allow us to fit sigmoidal shape to similar curves with the following actions and tendencies:

- k is acting on the amplitude gap of the normalized sigmoidal function, where asymptotic level at $x \gg 0$ arises to k.
- A allows the sigmoid curve to shift among the x-axis.
- r is the parameter that modifies the global slope of the sigmoid, with the inflexion point centered in $x = 0$.

We can identify and adapt the non-linear variation of curves of drain current I_{DS} among gate voltage V_{GS}, at a fixed output voltage V_{DS0}, to general sigmoidal equations, with the corresponding terms:

$x \cong V_{GS}$; $\sigma \cong I_D$; k, A and $r \cong$ set of values for each V_{DS} nominal fixed value (V_{DS0}).

$$I_{DS}(V_{GS})\Big|_{V_{DS0}} = \frac{k|_{V_{DS0}}}{1 + A|_{V_{DS0}} \, e^{-r|_{V_{DS0}} \cdot V_{GS}}} \tag{13}$$

An example of this fitting technique is presented in **Figure 6**, for one of the experimental curves $I_D(V_{GS})@V_{DS0} = 15$ V realized on a power SiC MOSFET [29].

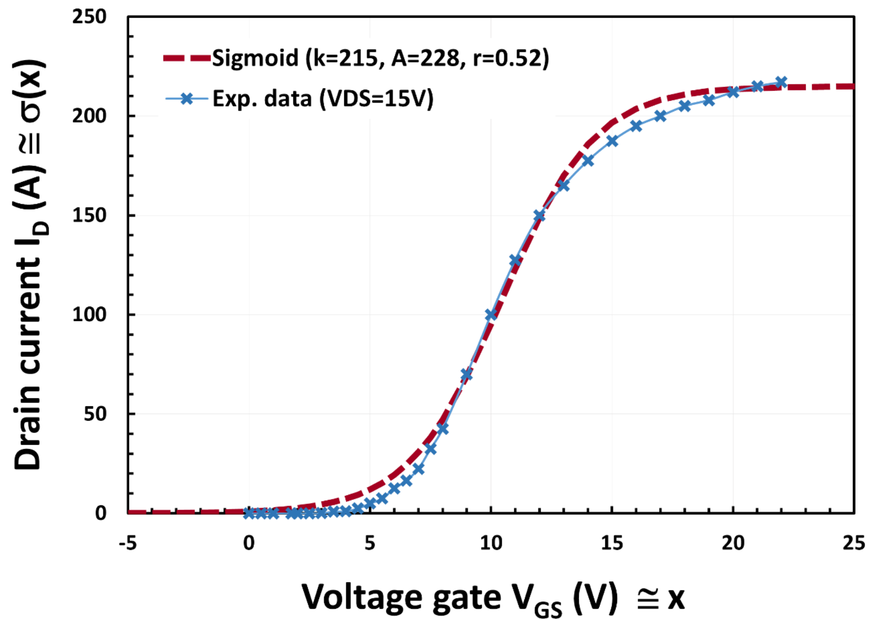

Figure 6. Example of identification of MOSFET transfer characteristic $I_D = f(V_{GS})$ with generalized sigmoid $\sigma(x) = \frac{k}{1 + Ae^{-rx}}$ ($k = 215$, $A = 228$, $r = 0.52$).

The following improvement we propose for electro-thermal modelling involves the temperature T dependency in the equations of current and voltage of the MOSFET transistor. Transconductance gm—*i.e.*, derivative of $I_{DS}(V_{GS})$ curve—is strongly impacted by thermal variations, with significant changes in slopes and current amplitudes in regions 2 and 3 of the output transfer characteristic. These shifts are commonly observed in SiC MOSFET responses when experimentally stressed by external steps of temperature, as the general typical shape of sigmoid is maintained [18]. We confirm these observations through our own experimental tests, as discussed in the following section of this paper. To fit these parametric curves, we propose to introduce some temperature-dependency expressions on the three parameters k, A and r of the sigmoid equation, valid at a single fixed output voltage V_{DS0}:

$k = k(T)$, $A = \alpha_2(T)$, and $r =$ constant. As mentioned previously, the r parameter has an impact on the slope of the sigmoid around the inflexion point, and experimental data of $I_D(V_{GS})$ with a large range of temperature (≈150˚C) show a very light variation of these slopes in region 2. So, we assume that r parameter stays very weakly dependent on T, and to keep its initial value determined at V_{DS0}.

Consequently, the temperature dependency of total current I_{DS} is proposed by

the modified equation:

$$I_{DS}(T) = \frac{k(T)}{1+\alpha_2(T)\mathrm{e}^{-r \cdot V_{GS}}} \tag{14}$$

where $k(T)$ and $\alpha_2(T)$ are polynomial expressions for temperature dependence of $I_{DS}(T)$, and r is the transconductance coefficient (V^{-1}).

The temperature influences the variation of the transconductance curve depending on the threshold voltage V_{GSTH}. In the case where $V_{GS} < V_{GSTH}$, with V_{GSTH} also depending on the temperature, the current source will supply any current (Cutoff mode). In other cases, in conduction mode, the equation of the drain current $I_{DS}(T)$ is used. To consider the thermal dependence at different values of the voltage V_{GS}, the following expressions for the polynomial equations of $\alpha_2(T)$ and $k(T)$ are proposed:

$$\alpha_2(T) = \phi_1 \cdot T + \theta_1 \cdot T^2 + \sigma_1 \cdot T^3 + \varpi_1 \tag{15}$$

$$k(T) = \phi_2 \cdot T + \theta_2 \cdot T^2 + \sigma_2 \cdot T^3 + \varpi_2 \tag{16}$$

The equation of $\alpha_2(T)$ is useful to maintain the regular linear variation of the I_{DS} variation in region 2, despite the temperature-induced changes. Equation of $k(T)$ is useful to handle the variation of the saturation level caused by temperature changes, in region 3 of the $I_{DS}(V_{GS})$ curve.

Finally, the whole behavioral model for the SiC MOSFET, including thermal dependencies with the representative equations of $R_{DSON}(T)$, $I_{DS}(T)$ and $V_{GSth}(T)$, has 18 parameters and coefficients, as resumed and listed in **Table 1**. For implementation, these parameters can be deduced from the thermally dependent characterizations performed by the user, with initial starting values from transistor datasheets. We describe in the next section the proposed equivalent thermal model of the temperature, based on a well-known Cauer network, to be coupled with the electrothermal model of the MOSFET.

Table 1. List of thermal-electrical parameters of the behavioral model of the SiC MOSFET.

Symbol	Quantity	Role
l_1	Drain resistance R_{DSON} temperature coefficient	1st *order*
l_2	Drain resistance R_{DSON} temperature coefficient	1st *order*
d_1	Drain resistance R_{DSON} temperature coefficient	2nd *order*
d_2	Drain resistance R_{DSON} temperature coefficient	2nd *order*
y_1	Drain resistance R_{DSON} temperature parameter	*zero order*
y_2	Drain resistance R_{DSON} temperature parameter	*zero order*
b_2	Threshold voltage V_{GSth} parameter	*zero order*
j_1	Threshold voltage V_{GSth} temperature coefficient	1st *order*
w_1	Threshold voltage V_{GSth} temperature coefficient	2nd *order*
r	Transconductance coefficient	-
v_1	Transconductance temperature parameter	*zero order*

Continued

v_2	Transconductance temperature parameter	*zero order*
f_1	Transconductance temperature coefficient	1st *order*
f_2	Transconductance temperature coefficient	1st *order*
q_1	Transconductance temperature coefficient	2nd *order*
q_2	Transconductance temperature coefficient	2nd *order*
s_1	Transconductance temperature coefficient	3rd *order*
s_2	Transconductance temperature coefficient	3rd *order*

2.3. Description of the Thermal Cauer's Model Adapted to SiC MOSFET Cell

Considering the temperature generation and heat propagation in semiconductor circuits and active chips, a well-known thermal network based on Cauer's methodology is used for electrical and thermal simulations in electrical systems [29]-[32]. The Cauer's model allows the internal temperature of the chip to be calculated at each step of time, as the current and voltage vary during the switching action of the semiconductor. The implementation of a Cauer's model consists of linking the thermal resistance, R_{th}, and thermal capacitance, C_{th}, to simulate and represent the static and dynamic variations of the temperature into the layers. Among the complexity of heat transfer between each layer of a physical structure, a set and number of cascaded R_{th}-C_{th} cells can be adjusted by the user, thus increasing the order of the simulation. This topology can be used in electrical circuit solvers, because of the analytical analogy between heat flow and electric flow, with temperature and thermal flux(power) equivalent to electrical potential (voltage) and current flux [18]. Using this network modelling, we can define an equivalent thermal cell R_{th}-C_{th} at each step of temperature often generated at the interfaces of the material layers into the structure of the transistor, as globally illustrated in **Figure 7**. For n thermal-layers to be considered in the propagation of heat, a general distributed cascaded circuit network with the n-subsequent cells [R_{th_n}-C_{th_n}] would correctly represent the thermal path and the transfer of temperature from the heat source (junction) to heat sink (case or radiator).

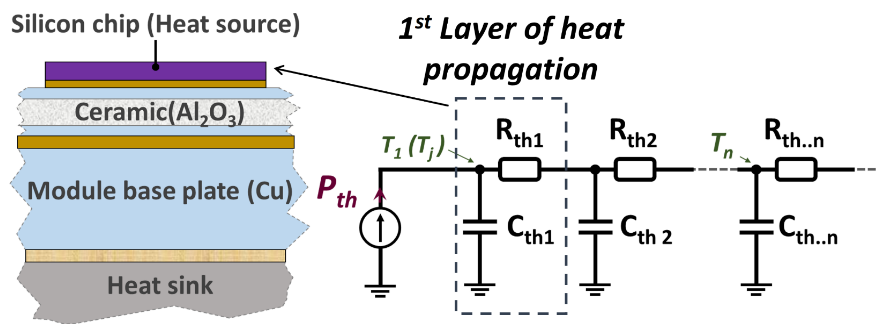

Figure 7. General thermal modelling of the different layers of a MOSFET transistor from semiconductor to radiator with Cauer's network topology.

To determine the values of R_{th_n} and C_{th_n} for each cell, the basic approach is to collect analytical and physical calculations of thermal quantities of different material and components. There is a consequent base of these data in literature, applications notes and manufacturer datasheets. But the user must have a very fine knowledge of physical construction and specific materials of the device in study. To an alternative without degrading the quality of the model for simulation, this analytic model of the thermal network can be extracted and adjusted with external characteristics of the heat transfer into the device. For this, thermal setups and parametric experimental procedures are installed with corresponding equipment, such as thermal oven and temperature sensors. Then, numerous statistical measurements are carried out to achieve voltage and current evolution of the chip as a function of time and forced temperatures. Some manufacturers give also sometimes these experimental curves, either in their device datasheet or at the ask. From these measured data, we can describe graphically the dynamic variation of the temperature ΣC_{th} as a function of the static variation ΣR_{th} (**Figure 8**). As this empirical curve shows successive linear variations in y-axis (C_{th}) and in x-axis (R_{th}), we can sample and model the thermal inertia and static features using paired values of the R_{th}-C_{th} cell, to the extent that they align with available experimental data.

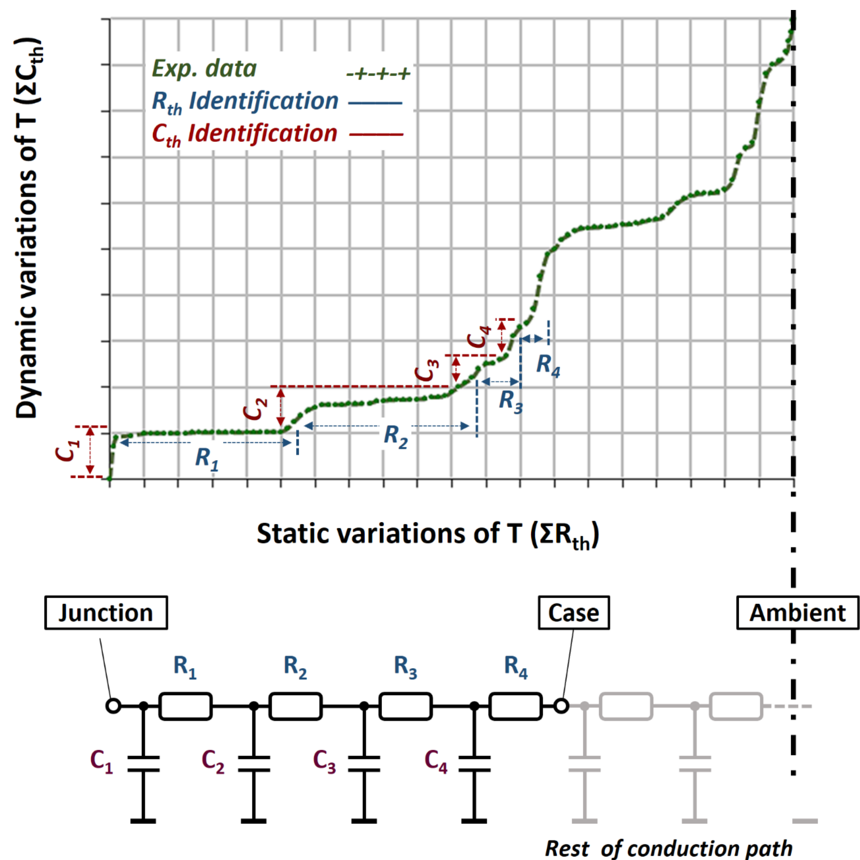

Figure 8. Example of R_{th}-C_{th} cell identifications with experimental thermal dependent data on a SiC MOSFET transistor.

The initial set of parameters is calculated with the first vertical shift among the y axis, that gives the value of C_{th_1}. Then, this value is maintained constant among the x axis until the next y shift, that identifies the R_{th_1} value. We obtain the successive numerical values of C_{th_j} and R_{th_j} among the successive Δy-Δx variations. We stop the extraction and validate the model at the n-order, with the end of data available which corresponds to the end of the heat conduction path (ambient temperature). Once defined and validated, this Cauer's network can be coupled with the electrical model in electrical solvers as Spice type, to complete the operational electrothermal model of the SiC MOSFET.

3. Implementation of the Electrothermal Model with a SiC MOSFET

In this section, the equations described above will be used to propose a complete procedure for implementing the whole behavioral model. We apply our method to a commercial SiC MOSFET from CREE, in TO-247 package [29]. For each equation, we need a set of initial values, obtained in most cases from the manufacturer's accessible data sheet. But in some cases of unavailable values due to confidential and innovative semiconductor technology, or when the operational conditions specified in the manufacturer's datasheet do not align with the user's requirements, it is essential to perform a custom characterization under specific parametric conditions. Firstly, with external measurements as a function of temperature, we have compared the simulated curves with the normalized experiment data, as recommended by the manufacturers in their application notes [31]. Once validated, we can perform electro-thermal characterizations under higher electrical and thermal conditions than the nominal ones, thereby extending the validity range of our model and enhancing the reliability of predictive simulations in challenging hard conditions for a power device.

3.1. Identification of $I_{DS}(V_{GS})$ with Genetic Algorithm Method

An optimization method is necessary to determine realistic values of the parameters and the coefficients of the non-linear variation of $I_{DS}(V_{GS})$ in (Equation (14)). For this, we propose a genetic algorithm concept, based on one of the currently available codes, called NSGA-II [33]-[35], and increasingly applied for numerical optimization in electrical and Multiphysics modelling procedures [36]. We have adapted this genetic algorithm to the sigmoidal function, representative of the similar behavior of $I_{DS} = f(V_{GS})$. To achieve this, dozens of parameters were initially generated, as the first step to meet the genetic algorithm requirements. The equation of I_{DS} is calculated with these values and is compared to the reference one. The difference between these two curves is denoted "Delta", that is a local criterion specific to NSGA method. The goal of the optimization procedure is to minimize the value of "Delta" (in %) at a stable quantity. Once the convergence of the Delta criteria is obtained for the first set of parameter values, this is the end of the step, and next iteration starts: a new set of samples are generated and in-

jected into the equation for a new calculation. This number of samples generated, for each step, is called "Design ID". These are reused to re-generate dozens of other possibilities, which iterate a new set and value of the Design ID. This process was repeated thousands of times until a combination of parameters was found to generate a curve almost identical to the reference one. For example, illustrated at **Figure 9**, the measurements of I_{DS} with V_{GS} ranging from 2 V to 30 V are compared to the calculations of the equation in the same conditions. After 4500 evaluations (Design ID), a correct configuration was obtained, with a stable value of error Delta < 20%.

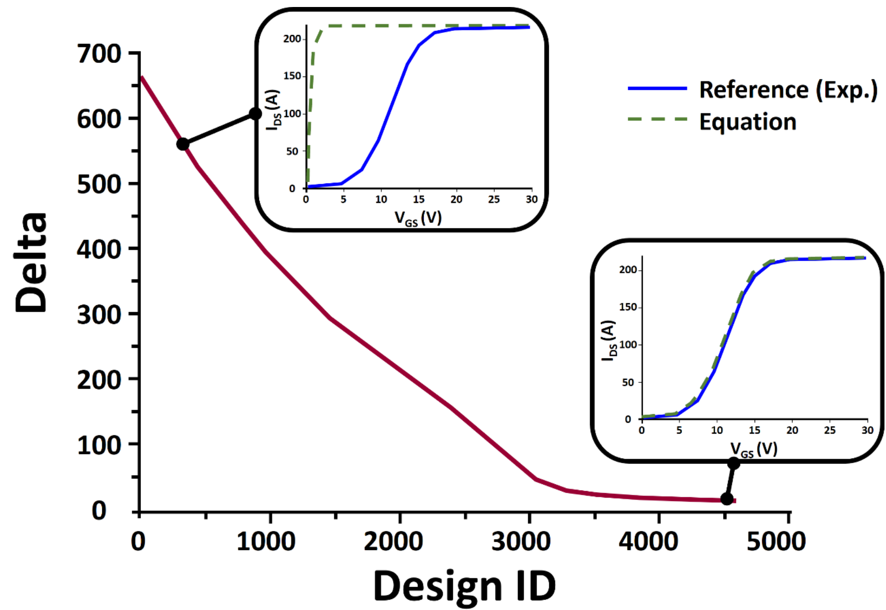

Figure 9. Optimization procedure with NGA algorithm for fitting calculated and experimental transconductance curves.

3.2. Identification of $I_{DS}(T)$ with RMS Algorithm

To consider now the identification of the multiple coefficients listed in **Table 1**, we have performed parametric electrical characterizations among the temperature on the SiC MOSFET demonstrator. The protocol consists of measuring the transconductance variations issued from transfer characteristics $I_{DS}(V_{GS})$ of the MOSFET chip beyond a set of temperatures from ambient to 200˚C, by using a dedicated setup with a steam room [31]. We can observe that the I_{DS} current value in the saturation region (V_{GS} = 20 V) has a high sensitivity with the temperature, with a negative coefficient of $\delta I_D/\delta T$. These variations show a shift from 215A@50˚C to 140A@175˚C. One of the parameters that have a numerical impact on the amplitude in the saturation region is the coefficient k of the sigmoidal function of I_{DS}. So, a reference curve of this $\delta I_D/\delta T$ is acquired by extracting the corresponding values of the drain current for a constant fixed voltage of the gate. This is illustrated on **Figure 10**, where this reference curve is extracted at V_{GS} = 20 V, with 5 points of I_{DS} for the 5 temperatures of the test.

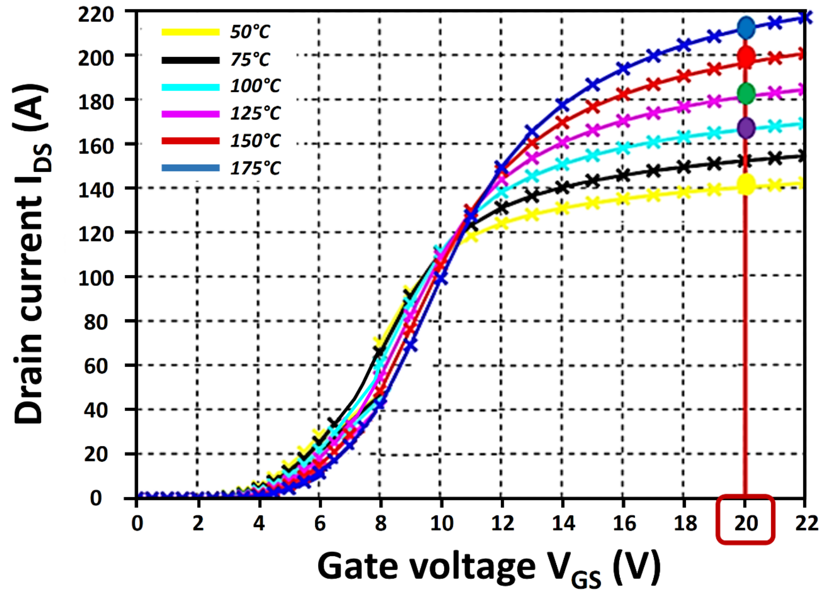

Figure 10. Characterization of the transconductance variations $I_{DS}(V_{GS})$ for the SiC MOSFET (CREE) from 50˚C to 175˚C (step of 25˚C)

From the graphical representation of these I_{DS} values among the temperature, in the saturation region where they are the more sensitive, we propose to define a polynomial equation, determined by linear regression [37], which can refine the precise calculation of the $\delta I_D/\delta T$ sensitivity (**Figure 11**). This operation with this interpolation will help to perform realistic electrothermal simulations over nominal activity range of the chip, for temperatures above 175˚C for example. This is the case when a short-circuit event is triggered, with the consequence of a sudden temperature runaway.

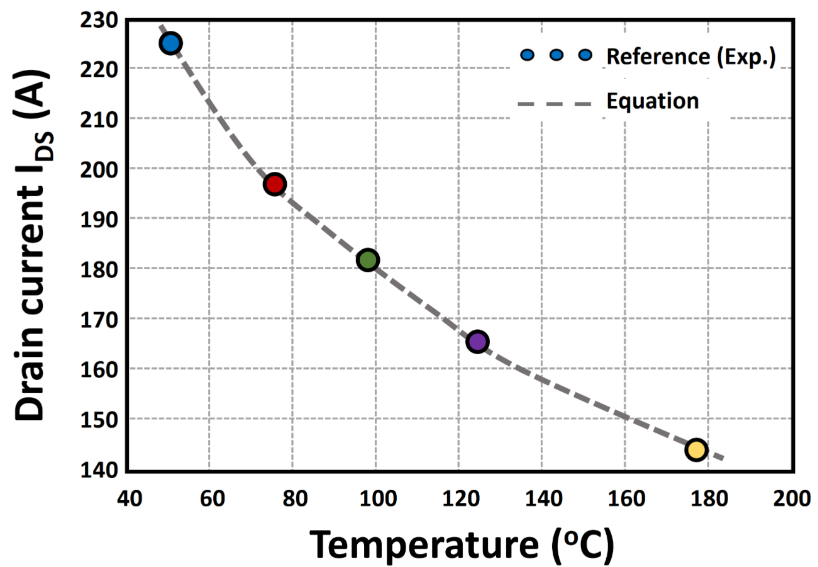

Figure 11. Determination of the curve for the thermal variation of drain current I_{DS} in saturation mode (V_{GS} = 20 V).

Once this curve is validated, we use a proprietary algorithm called RMS© (Root Mean Square) [36], developed from general theory of statistics [38]. It is adapted to complete the identification of all the parameters of the drain current equation in the formal sigmoid curve, incorporating the coefficients $k(T)$, r and $A(T)$. The global identification workbench includes optimization methods coupled with the genetic algorithm code described previously and the RMS calculations. **Table 2** presents the results of all the identification procedures we have conducted for the CREE SiC MOSFET transistor [29], including the values of the parameters and coefficients for their implementation in equations and in electrical circuit solvers.

Table 2. Calibrated model parameters and values for the SiC MOSFET CREE.

Symbol	Quantity	Value
l_1	Drain resistance R_{DSON} temperature coefficient	79.4n
l_2	Drain resistance R_{DSON} temperature coefficient	38µ
d_1	Drain resistance R_{DSON} temperature coefficient	1.84n
d_2	Drain resistance R_{DSON} temperature coefficient	754n
y_1	Drain resistance R_{DSON} temperature parameter	37.5µ
y_2	Drain resistance R_{DSON} temperature parameter	26m
b_2	Threshold voltage V_{GSth} parameter	3.02
j_1	Threshold voltage V_{GSth} temperature coefficient	−6.5m
w_1	Threshold voltage V_{GSth} temperature coefficient	5.49µ
r	Transconductance coefficient	0.536
v_1	Transconductance temperature parameter	540.1
v_2	Transconductance temperature parameter	750
f_1	Transconductance temperature coefficient	−6.94
f_2	Transconductance temperature coefficient	−0.75
q_1	Transconductance temperature coefficient	48m
q_2	Transconductance temperature coefficient	788n
s_1	Transconductance temperature coefficient	−130n
s_2	Transconductance temperature coefficient	−289n

3.3. Implementation of Capacitive Elements

To complete the electrical model for its dynamic feature during switching activity, and implement it in a Spice electrical circuit, we need to determine the values of the capacitive elements of the proposed model of the SiC MOSFET: C_{GS}, C_{GD} and C_{DS}. Typically, the values of these capacitances have non-linear variations with respect to the voltages applied to the transistor, and especially among the drain

voltage. They all present a straight decrease at low voltages V_{DS} and then trend to stabilize at a constant value with higher nominal value of the output voltage V_{DS}. The manufacturer or user can obtain these variations through single impedance characterization performed successively on the three pins of the transistors, using an impedance meter at frequencies around megahertz. In these cases, and in datasheets, we have access to external measurements of capacitance at the terminals of the device, that are normalized in the same conditions of impedance measurements:

- the measurement of input capacitance between gate and source, with output drain-source at 0 V in AC, gives the capacitance denoted Ciss:

$$C_{Gate\text{-}Source}\big|_{\widetilde{V_{DS}}=0\text{ V}} = Ciss\left(V_{DS_{DC}}\right) = C_{GS}\left(V_{DS_DC}\right) + C_{GD}\left(V_{DS_DC}\right) \tag{17}$$

- the measurement of output capacitance between drain and source, with input gate-source at 0 V in AC, gives the capacitance denoted Coss:

$$C_{Drain\text{-}Source}\big|_{\widetilde{V_{GS}}=0\text{ V}} = Coss\left(V_{DS_{DC}}\right) = C_{DS}\left(V_{DS_DC}\right) + C_{GD}\left(V_{DS_DC}\right) \tag{18}$$

- the measurement of reverse or transfer capacitance between drain and gate, source at 0 V in AC, gives the capacitance denoted Crss:

$$C_{Gate\text{-}Drain}\big|_{\widetilde{V_{S}}=0\text{ V}} = Crss\left(V_{DS_{DC}}\right) = C_{GD}\left(V_{DS_DC}\right) \tag{19}$$

For our purpose, as some initial and quasi-static values can be directly obtained by the datasheet of the transistor manufacturer, we perform some complementary capacitance characterizations, with our own test range, to refine these data. We especially want to observe the dependency of capacitances variations among temperatures, for thermal-electrical modelling of SiC MOSFET. At first, these tests confirm the typical non-linear variations among V_{DS} supply voltages of the MOSFET tested [29]. They show also that there is a very weak effect of the external temperature on their nominal curves. For example, as seen in **Figure 12**, the evolution of the capacitance Ciss, as a function of the output voltage V_{DS} over the nominal range of 0 - 1200 V, does not show significant deviations with the large temperature values applied, from 22˚C to 175˚C. Maximum shift between curves is about 2.6% around 80 V. Therefore, in first approach, we can neglect temperature dependency and directly import the capacitance static curve in our model, as a realistic non-linear variation of the capacitance only among V_{DS}. As the value of the capacitance is quite constant, 250 pF in the range of 500 V to 1200 V, some simplifications can be made in the model to optimize the calculations, using these constant values instead of the non-linear equation. But, in extremes conditions, outside the nominal activity of the chip at the limit of degradation or destruction of the chip, strong voltage variations and falls during a hundred nanoseconds (short-circuit mode), the complete non-linear equation of capacitance is needed to reproduce these realistic behaviors. This case is important to find a compromise between the robustness of our thermoelectric model and the complexity and time calculations.

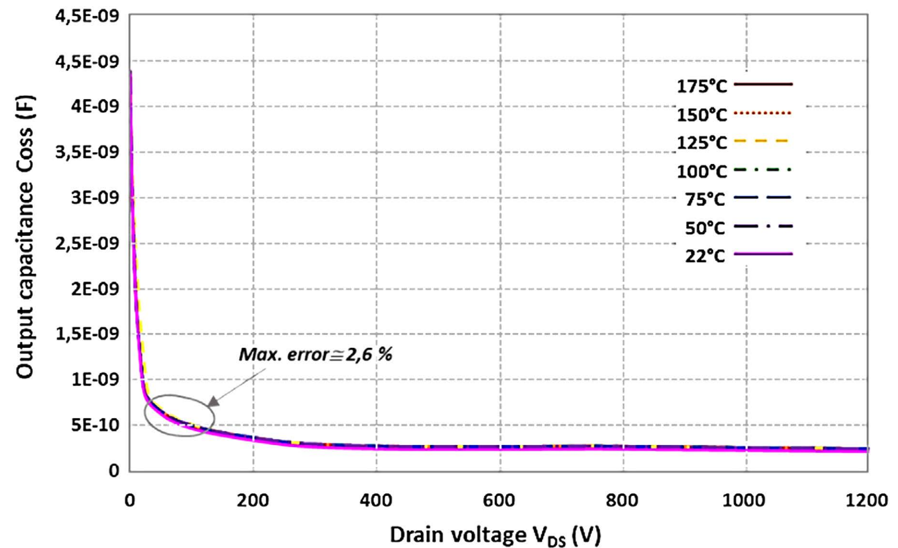

Figure 12. Evolution of Coss capacitance among supply voltage V_{DS} of SiC MOSFET CREE with different external temperatures.

4. Validation of the SiC MOFET Electrothermal Model

4.1. Topology of the Electrothermal Simulation

After calculating and implementing all the active and passive parameters of our model, based on a commercial SiC MOSFET [29], we confirm the validity domain of our model by comparing the deviation or the fit with the measurements. The experimental characterizations are based on recommendations of manufacturers in application notes [28]. We try to show that our compact model is compliant with these experiments, but also that it can rigorously simulate cases at the limits or outside the nominal activity of the ranges. In these cases, we can use it to indicate and reproduce severe conditions of limits of the switching activity of the SiC chips, short-circuit mode, and the consequences in terms of currents and temperatures that impact on chip reliability.

The thermal model based on Cauer's network is implemented as an equivalent circuit in a Spice-type solver (**Figure 13**), which has multi-domains links and algorithms to comply with both the electrical, high frequency and thermal calculations of circuits [39]. This temperature will be adjusted and calculated at each time step by the Cauer's model, with the input of the electric power supplied by the instantaneous values of V_{DS} and I_{DS}. In a first time, we define and start with the initial temperature of the Cauer's Model, T_0. The voltage and the current are calculated at this first step. With these values of $I_{DS}(t_0, T_0)$ and $V_{DS}(t_0, T_0)$, the equivalent power at the output of the chip $P_{th}(t_0)$ is coupled, as a heat flux source, at one terminal of the thermal model. A new value of the temperature of the junction is calculated. In a second step, this new temperature is fed into the electrical model, and the calculation is repeated until convergence and equilibrium of electrical power temperature. The calculation time will be proportional to the number of iterations until convergence (**Figure 13**).

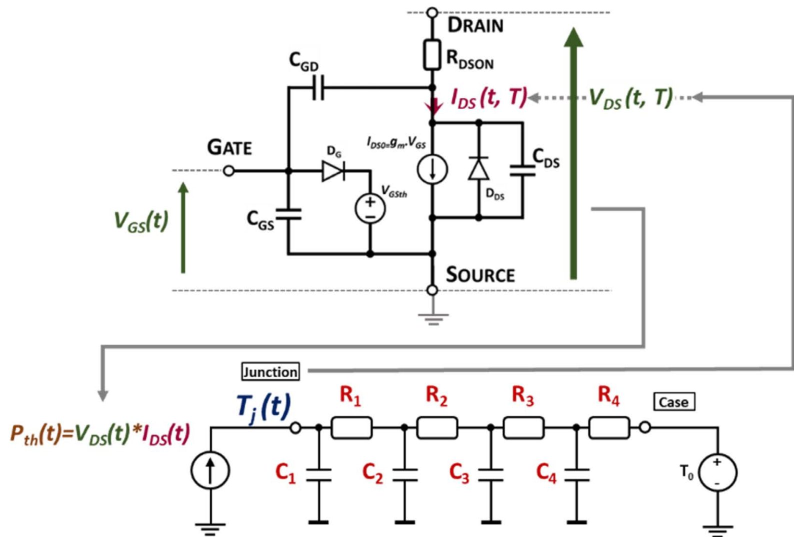

Figure 13. General schematic of the thermoelectric simulation couplings with Spice-multidomain solvers.

4.2. Validation of $V_{GSth}(T)$, $R_{DSON}(T)$ and $I_{DS}(T)$

The results and comparisons presented here are for the nominal and elevated temperatures defined during the characterization of the chip in thermoelectric test bench. First, the threshold voltage V_{GSTH} is represented with its temperature dependence, from ambient, 20˚C, to 175˚C. As seen in Figure 14, there is a good agreement of calculated values with measurement's data. The global error between simulation and measurements stays lower than 1% in the whole test temperature range.

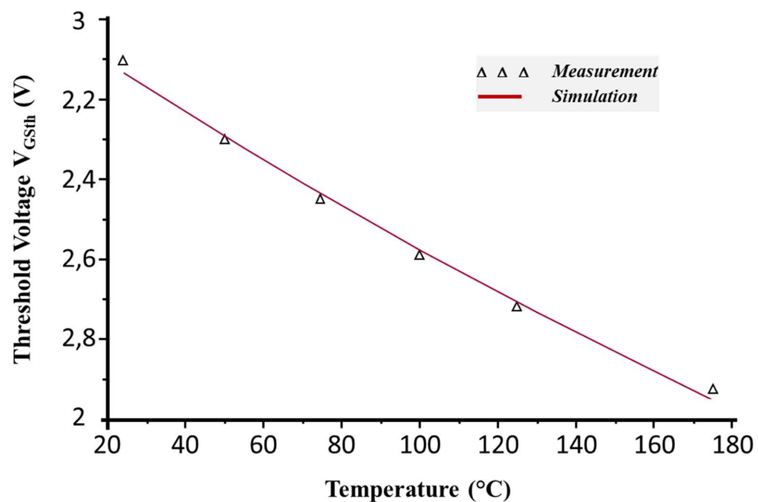

Figure 14. Comparison of the threshold voltage V_{GSth} of the SiC MOSFET CREE as a function of temperature, measured and simulated.

As this agreement is quite good, we can rely on Equation (4) of $V_{GSTH}(T^{\circ})$ for extra predictive simulation above 175˚C, to prevent high temperatures changes

and impacts on the electrical responses of the chip.

The second validation concerns the ON-state resistance R_{DSON} of the power MOSFET model, with its dependency to both electrical flux and heat flux. Experimental measurements of the drain resistance R_{DSON} on the industrial SiC MOSFET chip have been conducted in thermal test bench for different temperatures until 180˚C. These parametric characterizations confirm the shifts of R_{DSON} value, both with drain current I_{DS} and temperature (**Figure 15**). With drain current rise, drain resistance varies slightly and with very low linear slope. The variation is more pronounced with steps of temperature, for a fixed value of I_{DS}. At this figure, three curves at different temperatures (50˚C, 100˚C and 175˚C) are represented, to test and validate the R_{DSON} equation overall this range. We can observe that simulated and measured curves are in very good agreement, for a nominal range of current output up to 80 A, and for temperatures ranging from 50˚C to 175˚C.

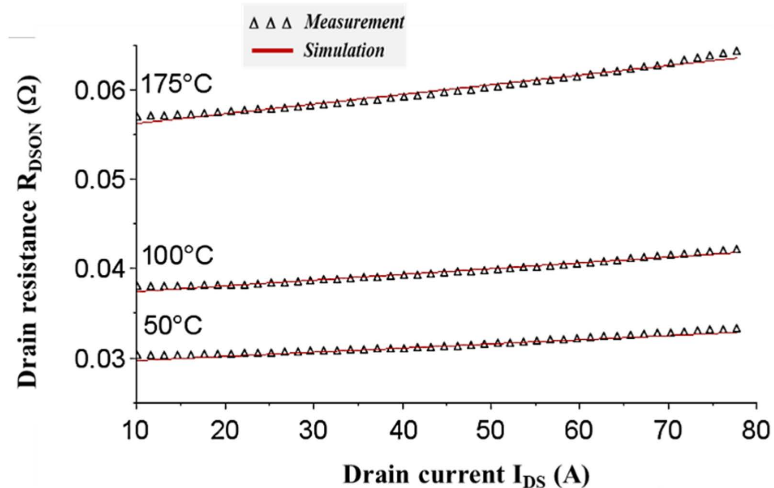

Figure 15. Comparison of resistance R_{DSON} variations at different temperatures, measured and simulated.

Finally, the main parameter with all non-linear electrical and thermal dependencies for a MOSFET, especially enhanced with SiC materials, is the transconductance g_m, derived from the $I_{DS}(V_{GS})$ non-linear curve. As mentioned, drain current $I_{DS}(T)$ is very thermal sensitive, due to the temperature dependency of parameters of its equation, as $V_{GSTH}(T)$. We compare, with all the set of parameters of the model identified in the previous section, the calculation of the I_{DS} variation and the equivalent transconductance with those of the measurements, for a conventional gate voltage range V_{GS} around 20 V for normal operation of the tested device [29]. Although there are some differences between the curves, especially in zone 2, it is mainly necessary to have a good simulation in zone 3, the saturation phase where the drain current is controlled and constant for switching in the nominal regime. As illustrated at **Figure 16**, we have a particularly good agreement of this level of current, for $V_{GS} > 20$ V, with the real measured one and at different temperatures.

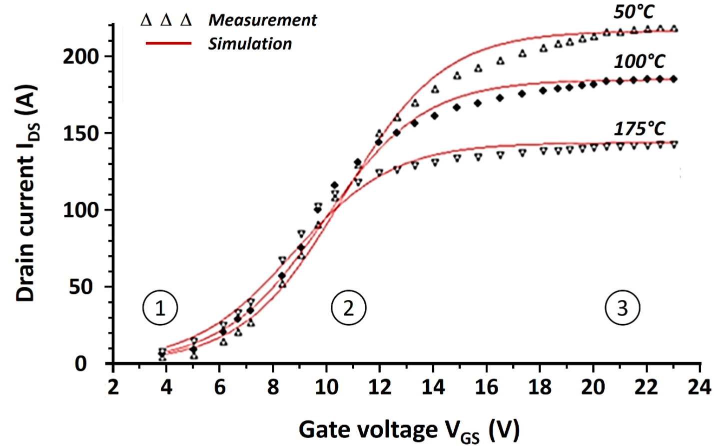

Figure 16. Comparison of variations of drain current I_{DS} as a function of the gate voltage V_{GS} for different temperatures.

These results confirm that the equation of $I_{DS}(T)$ can be considered as highly robust for the simulated phenomena. For extreme cases of chip activity, with local temperature reaching up to 200˚C, we can rely on these equations and the overall behavioral model to accurately predict the actual levels of current and temperature in the chip, as well as in the loads at 175˚C. As a reminder, the temperature in SiC MOSFETs during a short-circuit can reach up to 400˚C. We propose to evaluate simulations of the power chip under this short-circuit condition, focusing on high dI/dt and dynamic temperature conditions.

4.3. Application to the Short-Circuit Conditions of the SiC MOSFET

We complete the validity of our modelling methodology with the comparative simulation of short-circuit operation with experimental tests. To investigate the switching responses of the device during a short circuit, a validation board has been used [40]. This board includes short-circuit protection with appropriate driver functions. The measured chip was in a TO package with an *RDSON* equal to 25 mΩ and supplied by a *VDS* voltage of 600 V during the short circuit [41]. The parasitic inductances and other components of the board are considered in the simulation circuit, as given by the data of the package and of the board. Measurement and simulation in time domain of the evolution of the drain current $I_{DS}(t)$ with short-circuit operation occurring during 3 - 4 µs is represented at **Figure 17**. On the same figure, we represent on right y-axis the equivalent calculation of internal temperature varying during the rise of current density in the chip. We see a precise dynamic agreement between the two waveforms of the output current. Increase of current amplitude reaches a maximum value around 500 A, and then shutdowns, as internal temperature curve is continuously increased up to 41˚C. These current drops are due to parasitic impedances and the temperature rise, even if with a brief short circuit test in this test, the component does not have time to heat at a higher value. Therefore, in this case, we can confirm the validity of our modelling method for this component but also trust this thermoelectric model to

be used in limit or extra ranges of operation and give trusty internal information unavailable by the real tests [42].

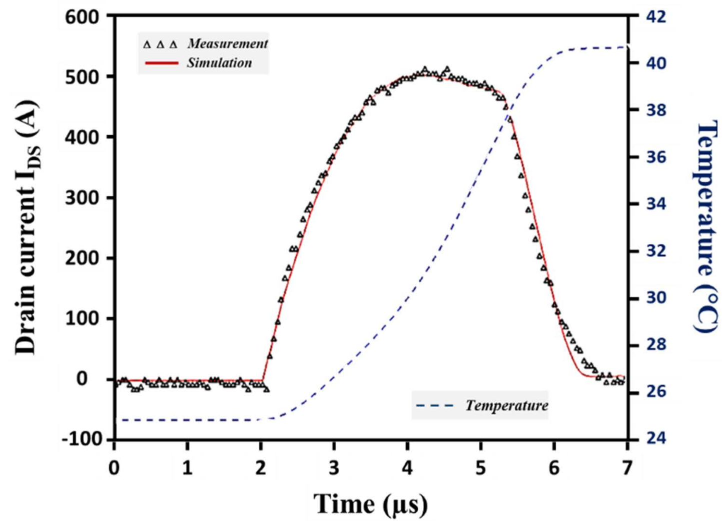

Figure 17. Comparison of the measured and simulated current and evolution of the temperature during a short-circuit.

5. Conclusions and Discussion

In this work, equation-based and behavioral modelling methods have been developed to propose confident electrothermal simulation of SiC power MOSFET devices, to be used within and outside operations for electrical supply applications. We have proposed to consider the thermo-dependence of the drain resistance *RDSON*, the transistor transconductance g_m and the threshold voltage *VGSth* with equations rigorously until the third order of temperature. The calculation and determination of the parameters and the coefficients of these equations, because of their substantial number (18), have also been performed with dedicated specific optimizations, as the genetic algorithm method developed for. With this electrical model of the SiC MOSFET, coupled to a Cauer's thermal network in a Spice-multidomain solver, the simulation of the performances and the limits of SiC MOSFET operations can be solved in a satisfactory time (≅seconds) with minimum error (<3%) to real features. The good concordances of time-domain waveforms between measured and simulated short-circuit currents at the output validate the use of this circuit model for a single SiC MOSFET chip in extreme conditions.

Since the identification process for this model was also based on experimental data outside the nominal range provided by datasheets, we believe that this model can assist in identifying the short-circuit duration required to induce the thermal impacts responsible for unwanted failures when used in commercial service. We aim to extend this study to encompass a complete power pack used for train traction. For this, the behavioral model of SiC MOSFET can be completed with packaging and routing connections RLC models, extracted from both experiments and

a quasi-static electromagnetic solver. We hope to propose robust and realistic calculations at a power module level and external output terminals, to simulate local hot spots of current, voltage and temperature. A key challenge of this work is the design of numerical twin models, allowing simulations to help predict levels of degradation and failures of power devices, thereby increasing the reliability and the understanding of SiC transistor lifetimes.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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